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Low-Power 200 MS/s 4-bit Flash ADC with Optimized Dynamic Comparator in 90 NM CMOS Technology

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ABSTRACT

In this paper, a low-power flash ADC has been designed and implemented in 90 nm CMOS technology with a supply voltage of 0.8 V. In the proposed flash ADC, a low-power double-tail dynamic comparator (DTDC) is utilized. With the addition of two PMOS transistors MR4 and MR5 to the DTDC's controlled reset phase, the internal nodes of the reset phase gradually discharge lowering the DTDC's power consumption, which in turn reduces the flash ADC architecture's overall power consumption. The important parameters have been studied through the simulation results in order to analyze the performance of flash ADC. The measured peak differential non-linearity (DNL) and integral non-linearity (INL) are +0.28/-0.37 LSB and +0.24/-0.43 LSB, respectively. With a 1.36 MHz input signal, the measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are 24.4 dB and 28.75 dB, respectively. The effective number of bits (ENOB) is 3.82 bits at 200 MS/s after the post layout simulation. It is found that the total footprint of the ADC architecture is 90*95 µm*µm. The overall power consumption is reduced to 45.3 $\%$ compared to existing work.

Keywords

Dynamic comparator, double-tail, low-power, MUX- encoder, flash ADC

1. INTRODUCTION

An analog-to-digital converter (ADC) is an essential component in low-power applications. It facilitates energy-efficient data transmission and efficient signal processing. By converting analog signals, such as temperature, pressure, or sound, into digital form, ADCs allow micro-controllers and digital circuits to handle data more efficiently since digital signal processing consumes less power than analog signal processing [1]. Comparator is the important circuit component in the designing of ADCs. The comparator compares an input voltage (V_{in}) with respect to a reference voltage (V_{ref}) and the output produces as high or low [2]. The performance of the ADC is greatly influenced by the type of comparator employed in its architecture. Comparators are mainly classified into two categories: static comparators, also known as non-clocked comparators, and dynamic comparators, also known as clocked comparators. The static comparators are used in the handheld electronic applications because it is operate at lower supply voltages [3]. Several techniques have been developed to improve the speed of the comparators, such as CMOS TIQ comparator [4], time-domain comparator [5], regenerative comparator [6] and latched voltage comparator [7]. The time domain comparators, it directly affects the performance of the comparator when the clock is unstable. The input signal voltage range will be limited because the regenerative comparator uses a positive feedback mechanism to amplify small changes in the differential input signal in order to produce large output signal values [8]. The clock frequency limits the latched voltage comparator's performance; thus, it is unable to process continuous time signals [9]. Differential comparators are usually used in precision ADC applications where accuracy and noise rejection are essential since they are specifically designed to handle differential input signals [10]. Clocked (dynamic) comparators have zero static power, lower average power, periodic power consumption, output updates only on clock edges, and are efficient for high-speed applications. They also work in two phases: reset and evaluation [11]-[15]. However, the designing of high-speed comparator becomes much more complex for the low supply voltages. For an n-bit resolution, a flash ADCs needed ($2^n - 1$) comparators, which might result in a large number of components at higher resolutions. Power efficiency is a challenging issue, particularly for battery-powered systems [16]. Flash ADCs are often limited to lower resolutions as a result of the exponential rise in power consumption resulting from increased number of comparators. The flash ADC with parallel architecture is the preferred option for achieving high speeds at low resolution. However, the primary factor limiting its accuracy is the offset voltage of comparators and pre-amplifiers [17]. The offset voltage is reduced by using an offset calibration and segmentation technique [18]. However, these designs are sensitive to process, voltage, and temperature (PVT) variations [19]-[24]. In this work, a 4-bit flash ADC is designed with low-power DTDC in 90 nm CMOS technology. The result of the ADC performance is compared in terms of power, and static and dynamic performance of ADC. The main objective is to enhance flash ADC performance with a higher Figure of Merit (FOM) and reduce power consumption without influencing PVT variations. Further, the paper is organized as follows: In the section II discussion about double tail dynamic comparators and low-power flash ADC. The simulation results of frequency spectrum, corner analysis and Monte-carlo analysis are discussed in detail in section III. Finally, the conclusion is provided in section IV.

2. FLASH ADC ARCHITECTURE WITH LOW-POWER DTDC

A 4-bit flash ADC has been developed using low-power double-tail dynamic comparator and a multiplexer-based encoder. The architecture of 4-bit flash ADC is shown in Figure 1. To design an ADC with a 4-bit resolution it requires 16 resistors (2^n for n = 4), 15 comparators ($2^n - 1$) and three 2:1 multiplexers. The reference voltage of each comparator differs from the other comparator by one LSB (resolution in volts). Hence, the LSB of the flash ADC is given in "Eq. (1).

$$LSB = \frac{(+V_{ref}) - (-V_{ref})}{2^N} \quad (1)$$

Where, $+V_{ref}$ is the maximum reference voltage, $-V_{ref}$ minimum reference voltage of the resistive divider network. As given in Figure. 1, each double-tail dynamic comparator generates a thermometer code as an output after comparing the input signal voltage with respect to the various reference voltages. The encoder converts the thermometer code to binary code, resulting in the final 4-bit digital output (b0, b1, b2, b3).

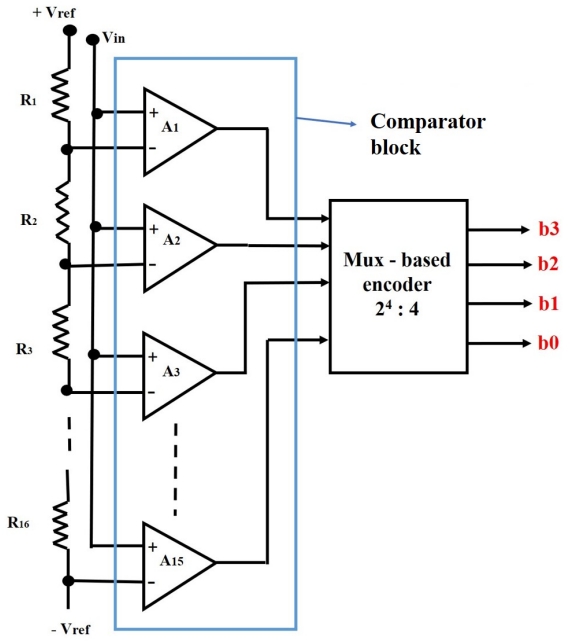

Fig. 1. Architecture of 4-bit flash ADC.

2.1 Low-Power DTDC

The comparator employed in the proposed ADC architecture has a lower input offset voltage and uses less power. Figure 2 shows a schematic diagram of DTDC. Transistors MC1 and MC2 in the pre-amplifier stage are cross-coupled to two parallel PMOS control transistors M3 and M4, result in improved comparator's latch speed. The transistors MR4 and MR5 are provided high-current path due to th large overdrive voltage that intended for achieving fast switching speeds. When clock (clk) is low, transistors Mtail1 and Mtail2 are turned off, while transistors M3 and M4 are turned on. This causes transistors MC1 and MC2 to turn off. At the same time, the pre-amplifier nodes Fn and Fp are connected to VDD. When MR4 and MR5 are turned off, the latch stage of transistors MR1 and MR2 activates, causing output nodes OUTp/OUTn

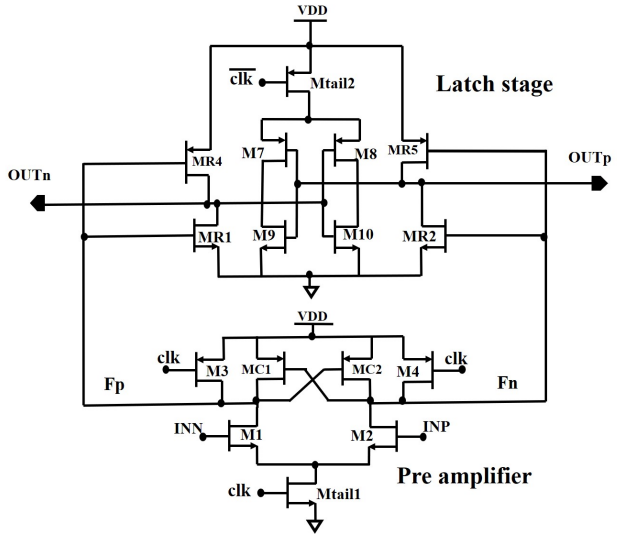

Fig. 2. Low-power double tail dynamic comparator.

to discharge to ground. At the regeneration phase, When clk is high transistors Mtail1 and Mtail2 turn on, whereas transistors M3/M4 turned off. The output nodes of the pre-amplifiers Fn and Fp begin to discharge from the VDD. If VINN $>$ VINP, the node Fn decreases faster than Fp due to the larger current of transistor M1 compared to M2. When Fn is consistently decreasing, transistor MC2 begins to turn on, causing the Fp node to return to VDD. Meanwhile, transistor MC1 remains off, allowing Fn to fully discharge. The response of nodes Fp and Fn is coupled to the positive feedback latch, which activates transistor MR5 and deactivates transistor MR4 as a result, the output nodes OUTn rapidly moved up to VDD and OUTp down to zero potential.

2.2 Multiplexer based Encoder

Multiplexers make signal routing and wiring in circuits easier. They make it easy to choose a single input from multiple sources, which reduces the interconnection network's complexity [25]. Multiplexers usually require less power than complex logic circuits, which can be useful in designs where power efficiency is an important consideration [26]. The architecture of 2:1 MUX-based encoder is shown in Figure 3. The relationship between the input lines, select lines, and output helps to construct a logical expression. Each output bit can be represented as an equation that specifies which inputs need to be active for the bit to be '1'. The logical equations for the output bits b_0, b_1, b_2, b_3 are given in "Eq. (2)", "Eq. (3)", "Eq. (4)", and "Eq. (5)"

$$b_3 = D_8 + D_9 + D_{10} + D_{11} + D_{12} + D_{13} + D_{14} + D_{15} \quad (2)$$

$$b_2 = D_4 + D_5 + D_6 + D_7 + D_{12} + D_{13} + D_{14} + D_{15} \quad (3)$$

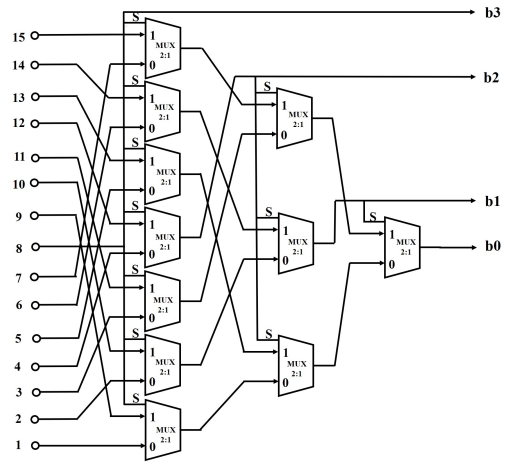

Fig. 3. Architecture of 16:4 bit MUX-based encoder.

$$b_1 = D_2 + D_3 + D_6 + D_7 + D_{10} + D_{11} + D_{14} + D_{15} \quad (4)$$

$$b_0 = D_1 + D_3 + D_5 + D_7 + D_9 + D_{11} + D_{13} + D_{15} \quad (5)$$

Only one of the encoder's sixteen inputs (D_0 to D_{15}) is active at a time (logic '1'). The output is chosen based on the combinations of the 16 inputs and logic gates which drive the MUX selection. MUX-based encoders can be economical in terms of component counts and total design cost because of their popularity and simplicity [27].

3. RESULTS AND DISCUSSION

A 4-bit flash ADC is designed and simulated in 90 nm CMOS technology. The performance of flash ADC is studied with a supply voltage of 0.8 V at sampling frequency of 200 MHz. Figure 4

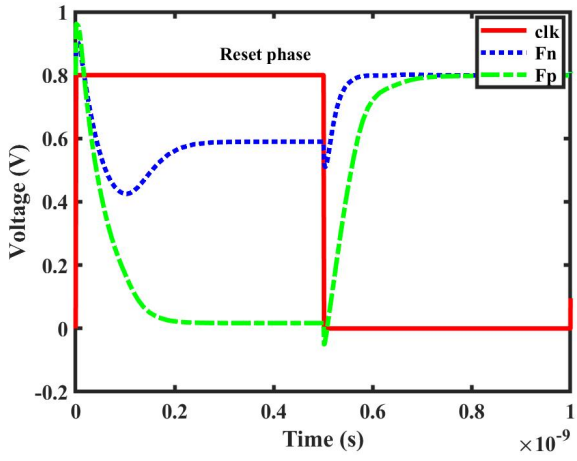

Fig. 4. Transient analysis of pre-amplifier stage DTDC.

illustrates the transient analysis of pre-amplifier stage of DTDC. It is showing when clk is high the output nodes of the pre-amplifiers Fn and Fp begin to discharge from the VDD. When VINP > VINN, the node Fp discahrge faster than Fn due to the larger current of M2 compared to M1. The Fn node return to VDD, when transistor MC1 begins to turn on. Meanwhile, transistor MC2 remains off, allowing Fp to discharge fully .

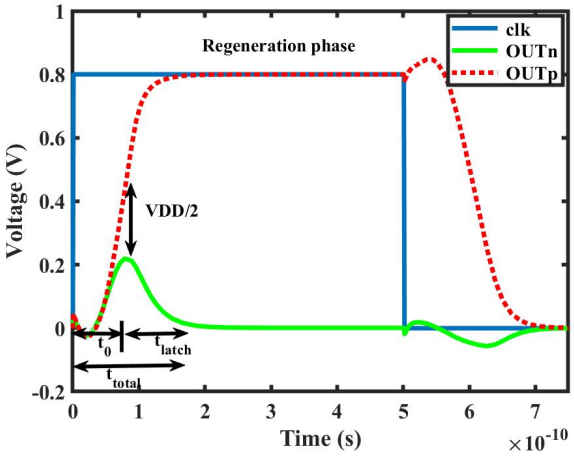

Fig. 5. Transient analysis of Latch stage DTDC.

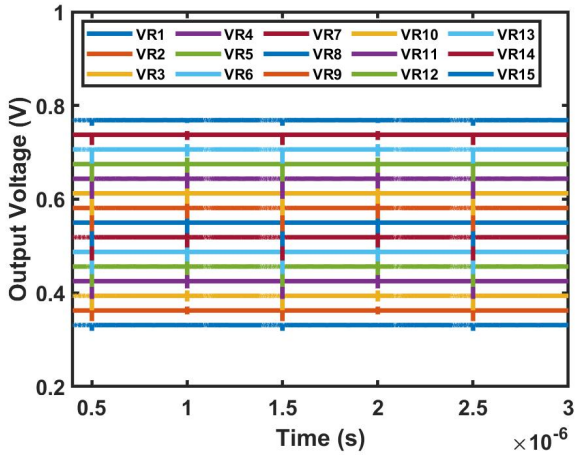

Fig. 6. Reference voltages of resistive divider network.

In the regeneration phase, the response of output nodes OUTp moved up to VDD and OUTn down to ground potential is shown in Figure 5. The different reference voltages produced by resistive ladder circuit is given in Figure 6. The reference voltages are generated from 0.331 V to 0.768 V with an equal interval. The flash ADC operates normally within the input signal dynamic range of 0.3 V to 0.8 V. The digital output waveform of the flash ADC is given in Figure 7. Digital code is generated from 0000 to 1111.
The DNL and INL of 4-bit flash ADC is shown in Figure 8 and Figure 9. DNL is measured at a maximum value of 0.28 LSB for

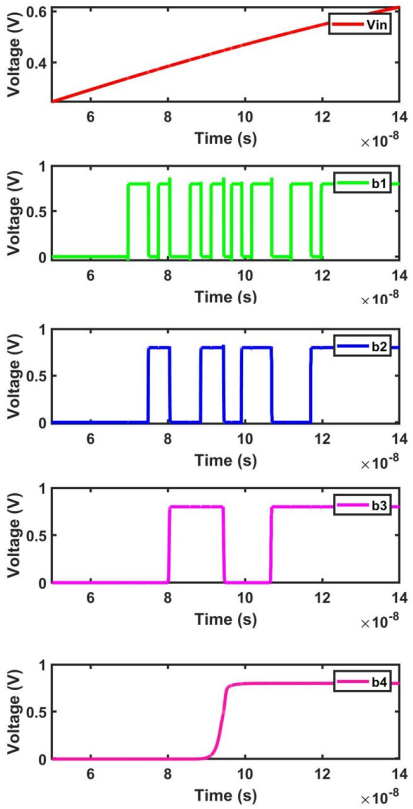

Fig. 7. Transient analysis of 4-bit flash ADC with an expanded output.

1000 output and at a minimal value of -0.37 LSB for 0111 output. Similarly, INL is measured for 0110 output at a maximum of 0.24 LSB and for 1010 output at a minimum of -0.43 LSB.

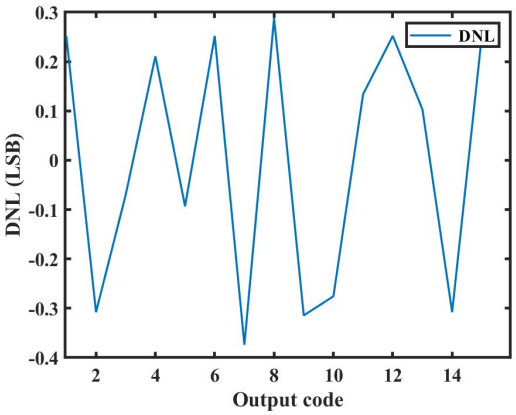

Fig. 8. DNL of 4-bit flash ADC.

To evaluate distortion and other important parameters such as SFDR and SNDR, a pure sine wave can be used as the input signal for analysing the dynamic performance of the ADC. The output waveform is transformed into its spectrum using the Fast Fourier

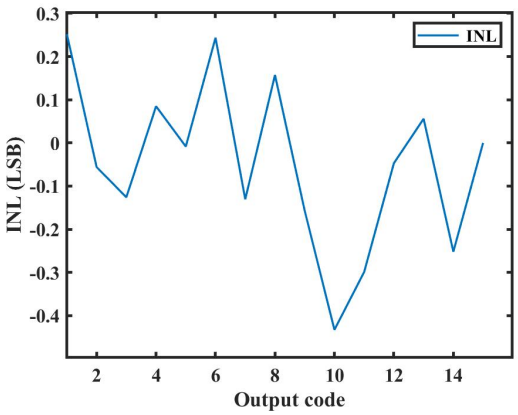

Fig. 9. INL of 4-bit flash ADC.

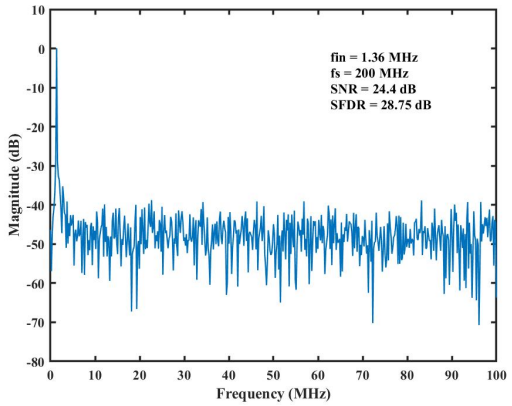

Fig. 10. The output spectrum at a sampling rate of 200 MS/s for input signal frequency of 1.36 MHz.

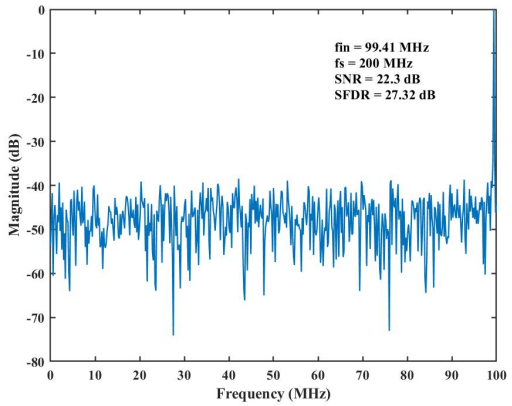

Fig. 11. The output spectrum at a sampling rate of 200 MS/s for Nyquist signal frequency of 99.41 MHz.

Transform (FFT). Figure 10 depicts the frequency spectrum of the flash ADC with an input signal frequency of 1.36 MHz and a sampling rate of 200 MS/s . The dynamic performance of the ADC is illustrated that, when input signal frequency is 1.36 MHz, the value of ENOB, SNDR, SNR and SFDR are obtained as 3.82 bits, 24.4 dB, 25.6 dB and 28.75 dB, respectively. Figure 11 shows the frequency spectrum of the flash ADC with a Nyquist input signal frequency of 99.41 MHz and a sampling rate of 200 MS/s . The obtained SNR is 23.3 dB with a 30.2 dB SFDR, SNDR is 24.8 dB and ENOB is 3.67 bits.

3.1 Monte-Carlo Analysis

Monte-Carlo analysis is performed to verify transistor mismatching and process variation realistically. Monte-Carlo simulations of DNL and INL for 200 runs after post-layout simulation is shown in Figure 12 and Figure 13. The standard deviations of DNL and INL are 0.26 LSB and 0.27 LSB, respectively.

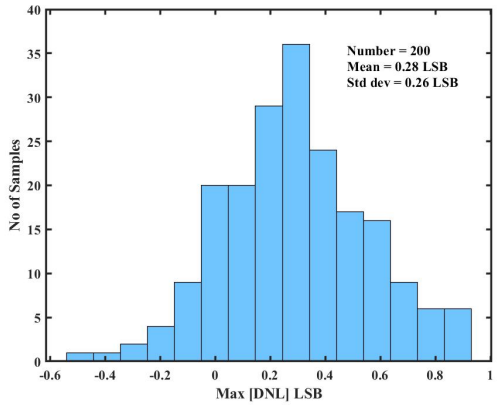

Fig. 12. Monte-Carlo analysis of DNL.

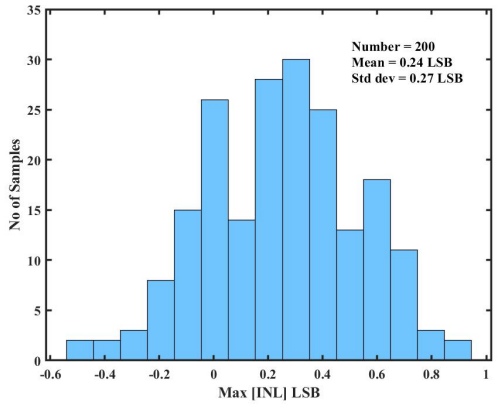

Fig. 13. Monte-Carlo analysis of INL.

Monte-Carlo analysis of SNDR and SFDR for an input signal frequency of 1.36 MHz is shown in Figure 14 and Figure 15. It is observed that the standard deviations of SNDR and SFDR are 0.27 dB

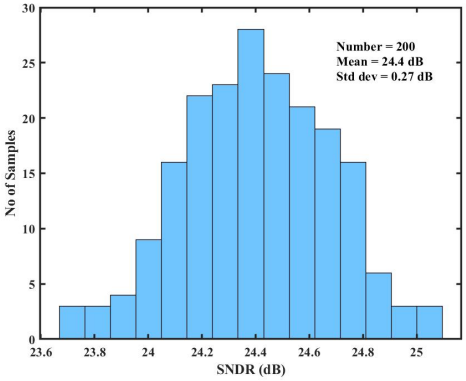

Fig. 14. Monte-Carlo analysis of SNDR with an input signal frequency of 1.36 MHz at 200 MS/s.

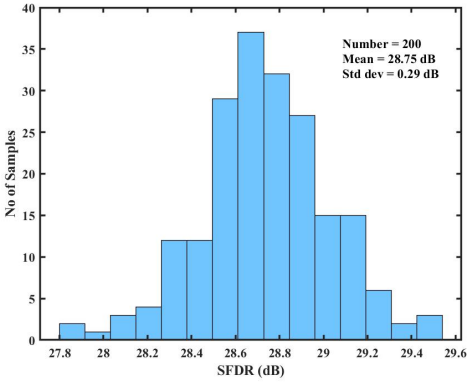

Fig. 15. Monte-Carlo analysis of SFDR with an input signal frequency of 1.36 MHz at 200 MS/s.

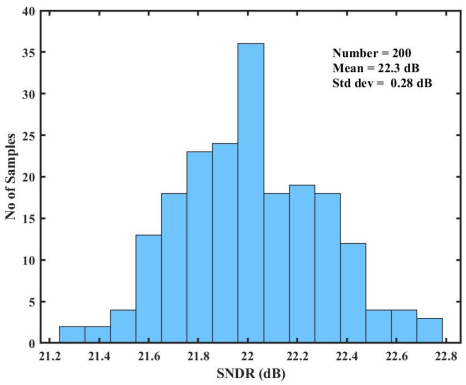

Fig. 16. Monte-Carlo analysis of SNDR with an input signal frequency of 99.41 MHz at 200 MS/s.

and 0.29 dB, respectively. Figure 16 and Figure 17 shows Monte-Carlo analysis of SNDR and SFDR for a Nyquist input signal frequency of 99.41 MHz. The standard deviations of SNDR and SFDR

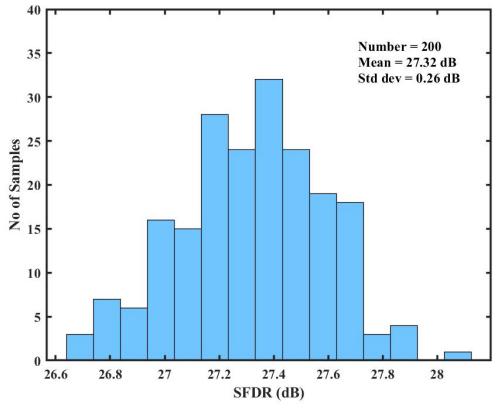

Fig. 17. Monte-Carlo analysis of SFDR with an input signal frequency of 99.41 MHz at 200 MS/s.

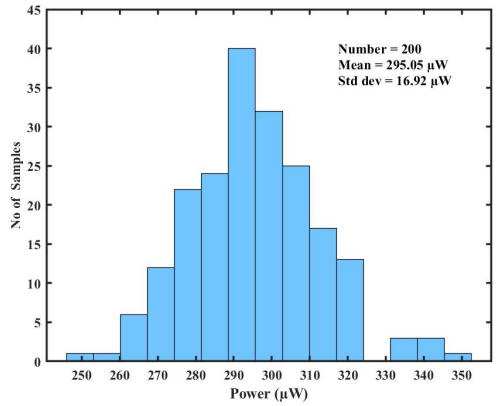

Fig. 18. Monte-Carlo analysis of total power consumption for 200 runs.

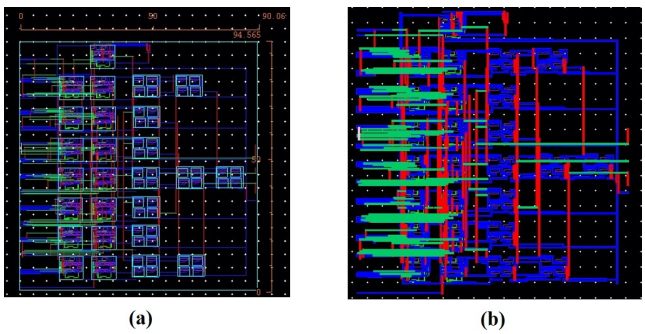

Fig. 19. Layout of 4-bit flash ADC (a) Pre-layout (b) Post-layout.

are found to be 0.28 dB and 0.26 dB, respectively. Monte-Carlo analysis of the total power is given in Figure 18. The standard deviations of power is 16.92 µW. The pre-layout and post-layout design is verified with help of design rule 90 nm technology. It has been found that the ADC architecture's overall footprint is 90*95 µm*µm. The post layout simulations are carried out and the same is used to confirm the DRC, LVS, and RCX of the whole flash ADC layout. Especially, a large mismatches and associated noise would significantly impair an analog circuit's performance in the absence of a proper layout. The layout and RC-extracted view (post-layout) is generated by the post-layout simulation is given in Figure 19 (a) and Figure 19 (b). Parasitic capacitance and resistors extracted from the layout are considered in the post layout simulations. It is observed that the double tail dynamic comparators power consumption is increased from 236.116 µW to 283.7 µW with the parasitic components. Similarly, the resistive ladder circuit power consumption is about 1.37 µW and the power consumption of the encoder is 9.96 µW. Furthermore, the overall power consumption is 295.05 µW for VDD = 0.8 V at 200 MS/s Nyquist sampling rate.

3.2 Corner Analysis

Corner analysis is carried out at various process corners SS, TT, SF, FS, and FF to determine the efficiency of NMOS and PMOS transistors. The simulations are carried out at different temperatures

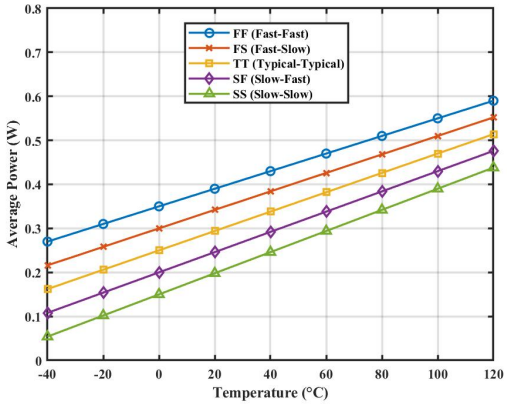

Fig. 20. PVT analysis of average power versus temperatures (T= -40° C to 120° C).

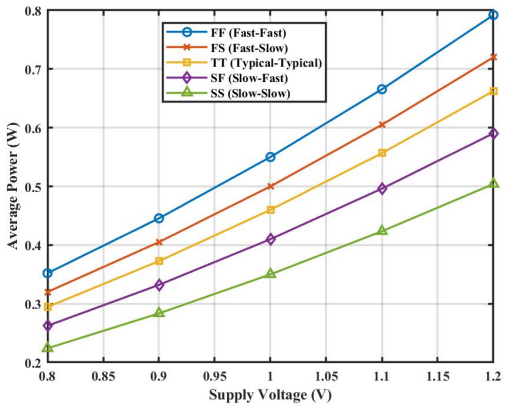

Fig. 21. PVT analysis of average power versus supply voltage (0.8 V to 1.2 V).

for various supply voltages in order to evaluate and ensure performance across a wide range of operating temperatures. Figure 20 shows as the temperature rises, power consumption increases gradually for every process corner. This is due to higher temperatures leading to greater dynamic power and leakage. At all temperatures, the FF corner consistently exhibits the highest power consumption, nearing 0.6 W to 0.7 W at 120° C. The SS corner exhibits the lowest power, varying from approximately 0.06 W at -40° C to 0.45 W at 120° C. Under these conditions, the relationship between temperature and power is indicated all curves are nearly linear.
Figure 21 depicts as supply voltage rises, so does power consumption in all process areas increases. Fast-Fast (FF) corner has the highest power consumption in comparison to other process corners. Typical-Typical (TT) corner consumes modest power. Slow-Slow (SS) corners have much lower power usage. The power usage is strongly correlated with the supplied voltage. Despite changes in absolute power amounts, the impact of voltage variations remains constant across all process corners. This graphic helps to guarantee that circuits will function effectively and securely under a range of manufacturing temperatures and conditions. It supports reliability evaluations, thermal analysis, and power budgeting.

3.3 Summary and Comparison

The overall performance of proposed design is summarized in Table 1. The performance of 4-bit flash ADC is improved in terms of figure of merit (FoM) and power consumption and the same are reduced significantly with the low power DTDC.

Table 1. Summary of flash ADC with proposed DTDC

Specification (unit)	Simulation Results
Technology (nm)	90
Supply voltage (V)	0.8
Resolution (bit)	4
Sampling frequency (Hz)	200 M
Inputdynamic range (V)	0.3 - 0.8
ENOB (bits)	3.82
SNR (dB)	25.6
SFDR (dB)	28.75
DNL (LSB)	+0.28/-0.37
INL (LSB)	+0.24/-0.43
Power consumption (μW)	295.05
FOM (pJ/con)	0.099
Area (μm *μm)	90*95

Table 2 illustrates the comparative study of 4-bit flash ADC with the existing work. The power is reduced to 45.3% compared to existing work [22]. FoM is improved to 0.099 pJ/conv, in comparison to previous work [23]. PVT analysis ensures that a proposed design meets the necessary performance requirements, including accuracy, power consumption, and robustness with regard to the variations in process, voltage, and temperature.

4. CONCLUSION

In this work, a 4-bit flash ADC with low power DTDC was presented. DNL and INL have been studied and found to be +0.28/-0.37 LSB and +0.24/-0.43 LSB which were well within the acceptable limits. With a 1.36 MHz input signal frequency, the measured SNDR and SFDR were 24.4 dB and 28.75 dB, respectively. Further, It was observed that the ENOB and FoM were significantly improved in the proposed design. The overall power consumption was reduced to 45.3 % compared to existing work. PVT analysis confirms that the proposed design was suitable for low-power applications.

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Table 2. Comparison to 4-bit flash ADC with reported works.

Parameters	[3]	[17]	[18]	[6]	[20]	[24]	[23]	[22]	This work
Technology (nm)	180	90	180	120	180	180	90	90	90
Supply Voltage (V)	1.8	1.2	1.8	1.8	1.8	1.8	1.2	0.35	1
Resolution (bit)	4	4	4	4	4	4	4	4	4
Sampling Rate (S/s)	3G	2.5G	1.6G	4G	700M	100M	1.2G	200M	200M
ENOB (bit)	3.89	-	4.4	-	3.77	3.62	-	3.03	3.82
Power Consumption (W)	505m	30m	15.5m	6.2m	5.56m	1.08m	2.5m	540 µ	295.05 µ
FoM pJ/conv	-	0.35	0.69	-	0.46	0.87	0.16	0.33	0.099

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