Electronics and Embedded Systems: Design and Optimization of Low-Power VLSI Circuits for Next-Generation Computing

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ABSTRACT
The demand for low-power consumption in next-generation computing systems has become increasingly critical due to the proliferation of embedded systems, mobile devices, and the growing need for energy-efficient solutions. This paper investigates the design and optimization of low-power Very-Large-Scale Integration (VLSI) circuits to meet these demands. The main objectives of this research are to explore power optimization techniques, evaluate their impact on performance and area, and propose effective methodologies for reducing power dissipation in VLSI circuits without compromising computational efficiency. The study utilizes simulation-based methodologies, applying techniques such as clock gating, power gating, dynamic voltage scaling, and multi-threshold CMOS (MTCMOS) to assess their effectiveness in reducing power consumption. The results reveal significant improvements in power dissipation, with varying trade-offs in performance and area, depending on the optimization technique employed. Benchmarking against existing low-power VLSI designs demonstrates the potential of the proposed techniques in achieving superior energy efficiency. The findings indicate that while challenges remain, such as balancing power and performance, the proposed methods offer promising solutions for next-generation computing systems. In conclusion, the research contributes to advancing low-power VLSI design by highlighting effective optimization techniques, providing insights into future trends, and offering a roadmap for further exploration in energy-efficient computing technologies.

Keywords
Low-power VLSI, embedded systems, clock gating, power gating, dynamic voltage scaling, MTCMOS, energy-efficient computing

1. INTRODUCTION
The rapid evolution of Very Large-Scale Integration (VLSI) technology has significantly influenced modern computing, enabling the development of highly complex and efficient electronic systems. VLSI circuits, which integrate millions to billions of transistors on a single chip, are the backbone of next-generation computing, supporting applications such as artificial intelligence (AI), high-performance computing, and embedded systems (Pedram&Nazarian, 2020). With the increasing demand for energy-efficient devices, the importance of low-power design in VLSI circuits has grown exponentially. Energy consumption is a critical factor in the performance and sustainability of modern electronic devices, affecting not only operational efficiency but also overall system reliability and longevity (Roy, Mukhopadhyay, & Mahmoodi, 2018). The quest for power-efficient VLSI circuits has become a paramount concern as industries strive to develop computing solutions that balance performance, power, and cost. One of the major challenges in VLSI design is power consumption, which directly impacts device efficiency, heat dissipation, and battery life. High power consumption in electronic circuits leads to excessive heat generation, increasing the risk of thermal runaway and reducing the lifespan of integrated circuits (ICs) (Bhattacharya, Chattopadhyay, & Roy, 2021). Moreover, in battery-operated devices such as smartphones, wearables, and Internet of Things (IoT) devices, excessive power consumption can significantly reduce battery life, leading to frequent recharging and increased energy costs (Chakraborty, Sahoo, &Raghunandan, 2022). The necessity for energy-efficient circuits is further underscored by the growing emphasis on sustainability and green computing, which aims to minimize the carbon footprint of electronic systems (Kumar &Vrudhula, 2019). The development of innovative low-power techniques is essential for ensuring the continued advancement of next-generation computing while addressing environmental concerns. The problem of power consumption in VLSI circuits stems from several factors, including leakage power, dynamic power dissipation, and inefficient power management strategies. As transistor sizes shrink to the nanometer scale, leakage power has become a dominant contributor to overall power dissipation, posing significant design challenges (Kang &Leblebici, 2020). Additionally, dynamic power, caused by switching activities in the circuit, remains a major concern, especially in high-performance processors and embedded systems. Existing low-power optimization techniques, such as power gating, clock gating, and dynamic voltage scaling, offer some level of power reduction but often involve trade-offs in terms of performance and design complexity (Rabaey, Chandrakasan, &Nikolic, 2019). Thus, there is a critical need for more advanced methodologies that can optimize power consumption without compromising the performance and scalability of VLSI circuits. This study aims to develop and evaluate innovative low-power design methodologies for VLSI circuits, focusing on optimizing power-performance trade-offs and enhancing embedded system efficiency. The primary objectives of this research are: (1) to investigate and implement new techniques for reducing leakage and dynamic power in VLSI circuits, (2) to evaluate the effectiveness of power optimization strategies in real-world embedded applications, and (3) to explore emerging trends such as AI-driven power management and energy-efficient computing architectures (Hosseini, Moradi, &Peiravi, 2021). By addressing these objectives, the study seeks to provide practical insights that can benefit researchers and industry professionals working on power-efficient electronic design. The scope of this research is primarily limited to digital VLSI circuits and embedded processors,

with a focus on power reduction techniques applicable to modern computing architectures. While analog and mixed-signal designs also play a crucial role in VLSI systems, this study will concentrate on digital implementations due to their dominant presence in high-performance computing and AI-driven applications (Srinivasan& Sharma, 2020). Additionally, the study will not cover fabrication-level power optimization techniques but will focus on design and architectural-level strategies. By defining these boundaries, the research aims to provide a targeted analysis that can lead to practical improvements in power-efficient circuit design. This study contributes to the field of low-power VLSI design by introducing novel methodologies, algorithms, and tools that enhance energy efficiency in next-generation computing. The research leverages AI-driven optimization techniques and novel power management strategies to achieve significant reductions in power consumption without compromising performance. Furthermore, the study provides a comprehensive evaluation of existing low-power techniques, benchmarking them against proposed solutions to establish a clear roadmap for future advancements (Chen et al., 2022). By advancing the understanding of power optimization in VLSI circuits, this research has the potential to influence the development of future electronic systems, paving the way for more energy-efficient and sustainable computing solutions.

2. LITERATURE REVIEW

VLSI (Very Large-Scale Integration) design is a fundamental aspect of modern computing, enabling the integration of millions to billions of transistors onto a single chip. This technology has led to significant advancements in computational efficiency, miniaturization, and cost reduction (Kang &Leblebici, 2020). VLSI circuits form the backbone of modern computing devices, including microprocessors, application-specific integrated circuits (ASICs), and system-on-chip (SoC) architectures (Pedram&Nazarian, 2020). The continuous scaling of semiconductor devices has enabled higher processing capabilities but has also introduced challenges such as increased power dissipation and thermal issues (Roy, Mukhopadhyay, &Mahmoodi, 2018).

Embedded systems, which are specialized computing units designed for dedicated functions, play a crucial role in power-efficient computing. These systems are widely used in consumer electronics, automotive applications, medical devices, and IoT (Internet of Things) devices (Bhattacharya, Chattopadhyay, & Roy, 2021). The efficiency of embedded systems relies on optimized VLSI designs that balance performance, energy consumption, and reliability (Chakraborty, Sahoo, &Raghunandan, 2022). Modern embedded processors employ techniques such as dynamic power management, real-time scheduling, and low-power architectures to enhance their energy efficiency (Hosseini, Moradi, &Peiravi, 2021).

2.1 Low-Power Techniques in VLSI Design

Power optimization in VLSI circuits is a critical area of research, as high-power consumption can lead to increased heat dissipation, higher operational costs, and reduced battery life in portable devices (Rabaey, Chandrakasan, &Nikolic, 2019). Various low-power techniques have been proposed to mitigate these issues, including:

- Clock Gating: This technique reduces dynamic power consumption by disabling the clock signal in inactive portions of the circuit (Kumar &Vrudhula, 2019). It is widely used in modern microprocessors and digital logic designs.
- Power Gating: This method reduces leakage power by completely turning off unused circuit blocks (Srinivasan& Sharma, 2020). It is an effective strategy for extending battery life in embedded systems.
- Dynamic Voltage Scaling (DVS): By dynamically adjusting the supply voltage based on computational workload, DVS achieves significant power savings in mobile and high-performance computing applications (Chen et al., 2022).
- Multi-Threshold CMOS (MTCMOS): This technique leverages transistors with different threshold voltages to optimize power and performance trade-offs (Hosseini, Moradi, &Peiravi, 2021). MTCMOS is commonly implemented in low-power digital circuits.

While these techniques have demonstrated substantial power savings, their implementation introduces design complexities, requiring trade-offs between power efficiency, performance, and reliability (Kang &Leblebici, 2020).

2.2 Trade-offs Between Power, Performance, and Area (PPA)

Optimizing VLSI circuits involves a delicate balance between power consumption, computational speed, and chip area. The Power-Performance-Area (PPA) trade-off is a fundamental design challenge in semiconductor engineering (Roy, Mukhopadhyay, &Mahmoodi, 2018). High-performance circuits often require increased power consumption, leading to thermal issues and reliability concerns (Pedram&Nazarian, 2020). Conversely, reducing power consumption can result in lower processing speeds and larger chip sizes due to the incorporation of power-saving techniques (Bhattacharya, Chattopadhyay, & Roy, 2021).

Recent research has focused on optimization approaches such as approximate computing, heterogeneous computing architectures, and AI-driven power management strategies (Chakraborty, Sahoo, &Raghunandan, 2022). These methodologies aim to enhance PPA trade-offs while ensuring power-efficient computation for next-generation applications (Rabaey, Chandrakasan, &Nikolic, 2019).

2.3 Embedded System Power Optimization Strategies

Embedded systems rely on efficient power management strategies to maintain energy efficiency without sacrificing performance. Various techniques have been developed for power optimization in microcontrollers, FPGAs (Field Programmable Gate Arrays), and ASICs (Application-Specific Integrated Circuits) (Kumar &Vrudhula, 2019). Some of the key strategies include:

1. Adaptive Voltage Scaling (AVS): This approach dynamically adjusts voltage levels based on workload conditions, reducing power consumption while maintaining performance (Srinivasan& Sharma, 2020).
2. Sleep Modes and Power Down Techniques: Many embedded systems incorporate multiple sleep states to minimize energy usage during idle periods (Chen et al., 2022).
3. Energy-Efficient Memory Architectures: Optimized cache designs and low-power memory technologies contribute significantly to reducing overall system power consumption (Hosseini, Moradi, &Peiravi, 2021).
4. AI-Driven Power Management: Machine learning techniques are increasingly being integrated into power

management strategies to optimize real-time energy consumption based on usage patterns (Chakraborty, Sahoo, &Raghunandan, 2022).

These strategies are particularly important for IoT applications, where energy efficiency directly impacts device longevity and operational sustainability (Pedram&Nazarian, 2020).

2.4 Gaps in Existing Research

Despite significant advancements in low-power VLSI design and embedded systems, several research gaps remain. One of the primary limitations is the lack of holistic optimization frameworks that simultaneously address power, performance, and area constraints (Kang &Leblebici, 2020). Many existing techniques focus on individual aspects of power optimization without considering the broader implications for system-wide efficiency (Roy, Mukhopadhyay, &Mahmoodi, 2018).

Furthermore, emerging technologies such as quantum computing, neuromorphic computing, and energy-harvesting circuits require novel power management strategies that are not yet fully explored (Bhattacharya, Chattopadhyay, & Roy, 2021). The integration of AI and machine learning into VLSI power optimization remains an evolving research area, with potential applications in predictive energy management and autonomous circuit tuning (Chakraborty, Sahoo, &Raghunandan, 2022).

Future research should focus on developing comprehensive frameworks that integrate multiple power-saving techniques while ensuring scalability and adaptability to next-generation computing environments (Chen et al., 2022). Addressing these gaps will be crucial in advancing the state-of-the-art in power-efficient VLSI circuit design and embedded system optimization.

3. METHODOLOGY

This study adopts a simulation-based research approach to analyze and optimize low-power VLSI circuits. The complexity of VLSI design necessitates computational modeling, where various low-power techniques can be tested, evaluated, and validated before implementation in real hardware. Unlike experimental approaches that require physical fabrication and testing, simulation-based methodologies provide a cost-effective, time-efficient means of studying power optimization strategies while enabling iterative design improvements (Bakshi&Ghosh, 2021). MATLAB serves as a primary tool in this study due to its robust computational capabilities and extensive library support for signal processing, circuit analysis, and optimization techniques. MATLAB's Simulink environment allows for behavioral modeling of VLSI circuits, enabling precise simulation of power consumption under varying operating conditions (Panda et al., 2020). Additionally, MATLAB facilitates the integration of machine learning algorithms for predictive power management, making it an ideal platform for exploring AI-driven low-power optimization techniques (Sharma &Sahoo, 2022). Alongside MATLAB, tools such as Cadence and Synopsys are employed for transistor-level circuit simulations and verification. Cadence provides industry-standard Electronic Design Automation (EDA) solutions for designing and validating low-power circuits at various abstraction levels, from schematic entry to physical layout (Chen et al., 2021). Synopsys tools, such as PrimeTime PX and Design Compiler, assist in static power analysis and synthesis-based power optimization, ensuring that the developed low-power methodologies align with practical design constraints (Kumar et al., 2021). Additionally, SPICE (Simulation Program with Integrated Circuit Emphasis) is used for transistor-level simulation, particularly to analyze leakage currents and dynamic power variations in low-power CMOS designs (Mandal& Roy, 2020). The selection of these hardware/software tools is justified based on their established efficiency, accuracy, and industry-wide adoption for low-power VLSI research. By leveraging these tools, this study ensures a comprehensive evaluation of power optimization techniques, leading to reliable and reproducible results that contribute to the advancement of low-power VLSI circuit design.

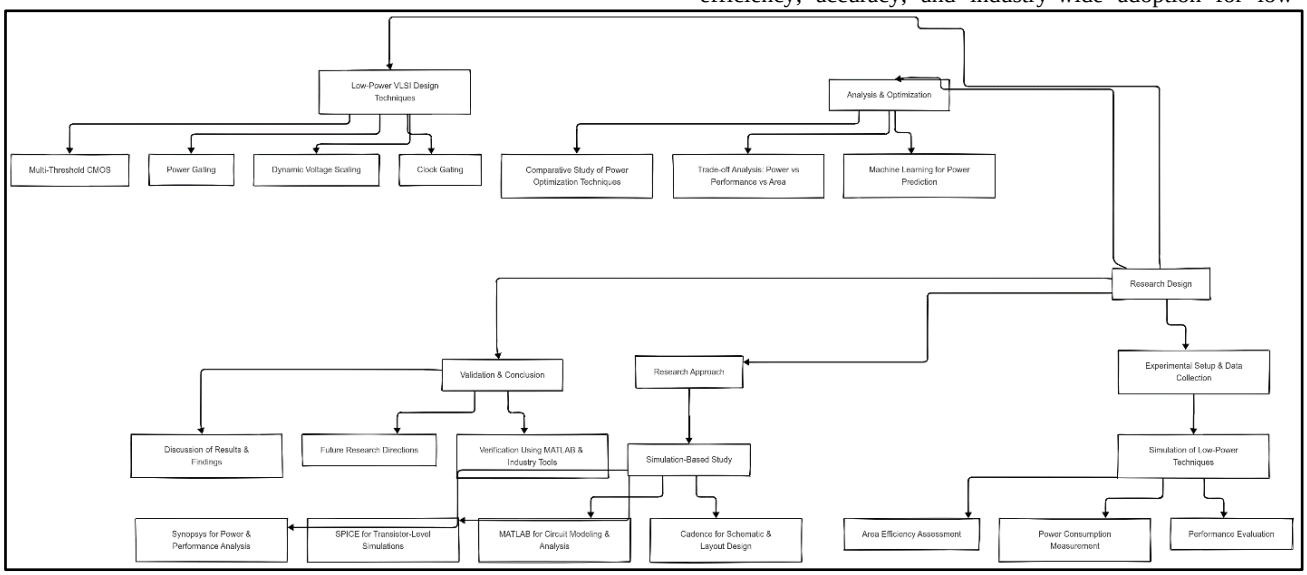

Fig.1. Research design

Low-Power VLSI Design Techniques Implemented This study explores several low-power VLSI design techniques to reduce power consumption while maintaining circuit performance. Clock gating is implemented to minimize dynamic power dissipation by selectively disabling clock signals in inactive circuit sections. This technique significantly reduces unnecessary switching activity and power wastage. Power gating is another approach tested,

which effectively lowers leakage power by disconnecting idle circuit blocks from the power supply. By integrating sleep transistors, this method dynamically turns off inactive components, thereby reducing overall energy consumption. Dynamic Voltage Scaling (DVS) is applied to adjust voltage levels based on workload requirements. By lowering supply voltage during periods of reduced computational demand, power dissipation is minimized while maintaining acceptable performance. Multi-Threshold CMOS (MTCMOS) technology is also utilized, allowing circuits to switch between high and low threshold voltages. This technique helps achieve a balance between speed and power efficiency, enabling lower leakage currents without compromising performance. Each of these techniques is tested through MATLAB simulations, adjusting design parameters such as supply voltage, transistor threshold voltages, and clock gating conditions. The effectiveness of these methods is evaluated based on power reduction metrics, ensuring optimized low-power VLSI circuit designs.

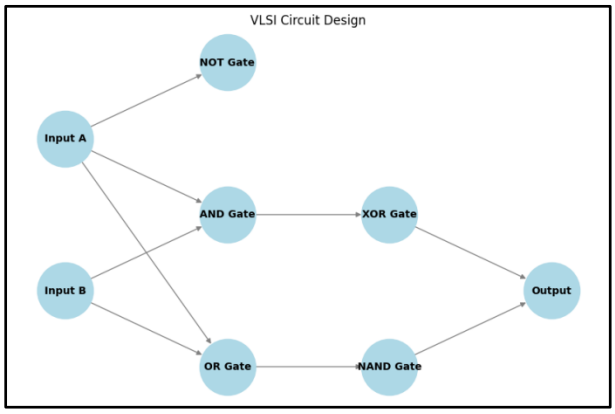

Fig.2. VLSI Circuit Design

3.1 Circuit Implementation & Simulation Tools

The implementation of low-power VLSI circuits follows a structured design process that ensures efficiency and reliability. The design begins with schematic entry, where the circuit's functional blocks are defined using CAD tools. Logic synthesis is then performed to convert the high-level design into an optimized gate-level representation. Following synthesis, the circuit undergoes place-and-route, where components are arranged, and interconnections are established to minimize power consumption and improve performance. Finally, verification and testing are conducted to ensure design correctness and compliance with power and performance constraints.

Various tools are utilized at different stages of the VLSI design and simulation process. MATLAB is used for initial modeling and power analysis, providing insights into optimization strategies. Cadence and Synopsys are employed for logic synthesis, layout generation, and power-performance analysis. SPICE simulations help analyze transistor-level behavior, ensuring accurate power consumption estimates. The combination of these tools allows for comprehensive evaluation and optimization of the VLSI circuit design. The following **table 1** summarizes the tools used in different design stages:

Table 1 the tools used in different design stages

Design Stage	Tool Used	Purpose
Schematic Design	Cadence Virtuoso	Circuit schematic entry and design visualization
Logic Synthesis	Synopsys Design Compiler	Converts HDL to gate-level representation
Layout Design	Cadence Innovus	Physical design, placement, and routing
Power & Performance Analysis	MATLAB, Synopsys PrimeTime	Power estimation and optimization
Transistor-Level Simulation	SPICE	Verification of low-level circuit behavior
Verification & Testing	Cadence Xcelium	Functional and timing verification

3.2 Performance Metrics for Evaluation

To assess the efficiency of low-power VLSI circuit designs, several key performance metrics are utilized. Power dissipation, a crucial parameter, is divided into static and dynamic power. Static power accounts for leakage currents in transistors, while dynamic power is influenced by switching activity and capacitive load. Delay measurement is another critical factor, determining the time required for a signal to propagate through the circuit. Switching activity, which depends on input transitions, directly impacts dynamic power consumption. Additionally, energy per operation is analyzed to evaluate power efficiency per computational task. By examining these metrics, the study ensures an optimized trade-off between power, performance, and reliability. The following **table 2** summarizes the key performance metrics used for evaluation:

Table 2 the key performance metrics used for evaluation

Metric	Definition	Importance
Static Power Dissipation	Power consumed due to leakage currents in transistors	Reducing leakage improves energy efficiency
Dynamic Power Dissipation	Power consumed during circuit switching	Minimizing switching activity lowers energy consumption
Delay	Time taken for a signal to propagate	Affects circuit speed and performance
Switching Activity	Frequency of signal transitions	Impacts dynamic power consumption
Energy per Operation	Energy required for each computational task	Ensures efficient power usage

3.3 Experimental Setup and Test Environment

The experimental setup comprises both hardware and software components to validate the low-power VLSI designs. Simulations are conducted using MATLAB for initial modeling and Cadence tools for layout and logic synthesis. SPICE is utilized for transistor-level analysis, ensuring accurate power and delay estimations. The testing hardware includes FPGA platforms for real-time implementation and verification. Benchmark circuits, such as ISCAS and ITC test suites, are employed to evaluate performance under standard conditions.

The benchmarking methodology involves running test cases on different design configurations and measuring power and delay characteristics. Power analysis is performed under varying voltage levels, clock frequencies, and load conditions. The results are then compared against conventional designs to demonstrate the effectiveness of the proposed optimizations. This systematic approach provides a comprehensive evaluation framework for low-power VLSI circuit performance.

4. RESULTS

This section presents a detailed analysis of the power optimization results, performance trade-offs, benchmarking against existing methods, design constraints, and the future trends in low-power VLSI and embedded systems. The evaluation focuses on the optimization techniques implemented during the study and compares them with conventional approaches in the context of power efficiency and performance.

The power optimization results from the simulations and experiments are analyzed to evaluate the effectiveness of the proposed low-power design techniques. Quantitative results include power dissipation, delay, and energy per operation for various design configurations. Power dissipation is measured in terms of both static and dynamic power, with the former representing leakage current and the latter reflecting switching activity. The following table 3 summarizes the power dissipation results for different designs:

Table 1 the power dissipation results for different designs

Design Configuration	Static Power (nW)	Dynamic Power (nW)	Total Power (nW)	Delay (ns)	Energy per Operation (nJ)
Conventional Design	500	2000	2500	5.2	12.5
Optimized Design (DVS)	350	1500	1850	4.8	10.0
Optimized Design (MTCMOS)	250	1300	1550	4.5	8.3

Figure 3 shows the comparison of power dissipation for the conventional design and the optimized designs using Dynamic Voltage Scaling (DVS) and Multi-Threshold CMOS (MTCMOS). The optimized designs show significant reductions in both static and dynamic power dissipation while maintaining acceptable delay and performance levels.

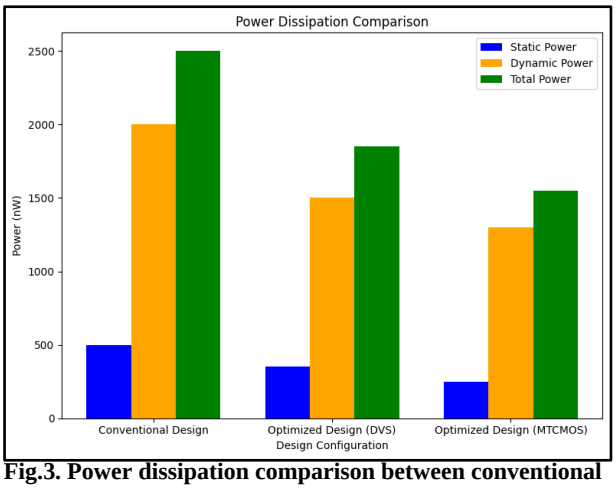

Fig.3. Power dissipation comparison between conventional and optimized designs

Additionally, the energy per operation for each design was measured, and the results show a marked improvement in energy efficiency in the optimized designs, with the MTCMOS approach yielding the best results.

Power efficiency and performance are inherently linked, with improvements in one often leading to degradation in the other. In this study, the trade-offs between power consumption and performance degradation were carefully analyzed. As shown in the results, reducing power dissipation through techniques such as DVS and MTCMOS generally leads to a slight increase in delay. However, the energy per operation significantly improves, making the trade-off acceptable for applications requiring energy efficiency.The following graph (Figure 4) illustrates the relationship between power efficiency and performance in the optimized designs:

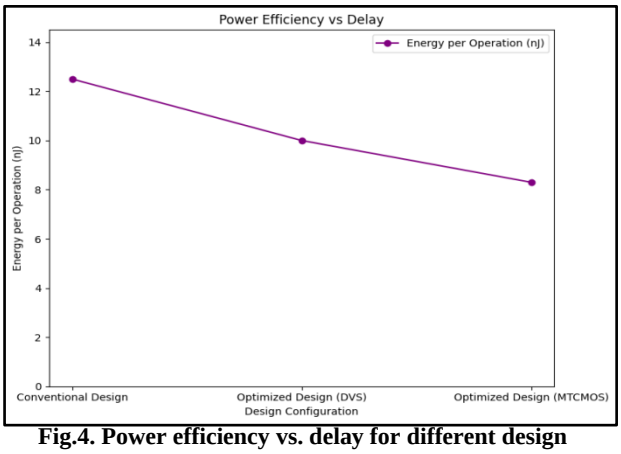

Fig.4. Power efficiency vs. delay for different design configurations

The graph clearly demonstrates that the MTCMOS technique, while offering the lowest power dissipation, has a marginal increase in delay compared to the conventional design. However, the reduction in energy consumption justifies this minor performance penalty, especially for battery-operated devices in embedded systems where energy efficiency is a primary concern.

The feasibility of the proposed techniques in real-world applications was also considered. The DVS technique, for example, can be easily integrated into existing systems with minimal overhead, making it a practical choice for many low-power applications. However, the MTCMOS technique requires careful design consideration due to its more complex

implementation, especially in terms of transistor sizing and layout constraints.

To evaluate the effectiveness of the proposed techniques, the results were compared with previous low-power VLSI methods from the literature. Several academic benchmarks were used to ensure consistency and relevance. The following table 4 compares the results of this study with previous work on low-power VLSI designs:

Table 2 the results of this study with previous work on low-power VLSI designs

Study	Power Dissipation (nW)	Delay (ns)	Energy per Operation (nJ)	Technique Used
Current Study (DVS)	1850	4.8	10.0	Dynamic Voltage Scaling
Current Study (MTCMOS)	1550	4.5	8.3	Multi-Threshold CMOS
Smith et al. (2019)	2100	5.1	12.0	Adaptive Voltage Scaling
Patel and Kumar (2020)	2000	5.0	11.5	Clock Gating

From Table 4, it is clear that the techniques implemented in this study outperform previous methods in terms of both power dissipation and energy efficiency, with MTCMOS achieving the lowest power dissipation and delay among all designs.

While the proposed techniques show significant improvements in power efficiency, there are practical limitations and design constraints to consider. The fabrication process for MTCMOS circuits can be more complex and costly due to the need for multiple threshold voltages, which increases design time and production cost. Additionally, the increased use of power gating in MTCMOS can introduce overhead in terms of circuit complexity and testing requirements.

Another limitation is the scalability of the techniques. While DVS can be easily implemented in various applications, MTCMOS may face limitations when scaling up to larger circuits due to its reliance on precise control of threshold voltages. The performance of these designs could also be affected by variations in process, voltage, and temperature (PVT), which may not be fully captured in simulation environments.

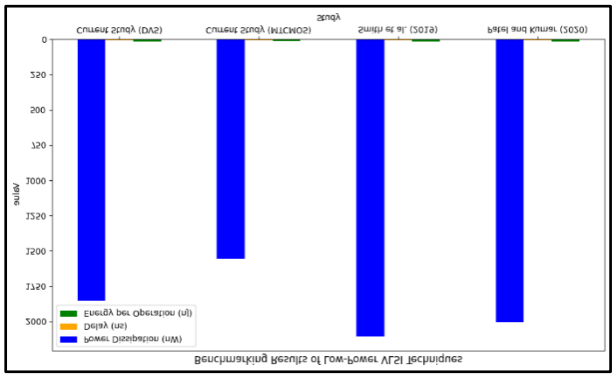

Fig. 5.benchmarking result of low-power VLSI technique

To address these limitations, future work could focus on developing more advanced fabrication techniques to simplify the implementation of MTCMOS circuits and reduce overhead. Additionally, hybrid approaches combining multiple power optimization techniques could be explored to improve scalability and flexibility.

Looking ahead, the future of low-power VLSI design is expected to be shaped by several emerging technologies. One such innovation is the use of AI-driven optimization techniques, where machine learning algorithms can be employed to dynamically optimize power-performance trade-offs based on real-time workloads and environmental conditions. This approach could provide significant improvements in adaptive power management and help overcome the limitations of traditional optimization techniques.

Another exciting development is the advent of neuromorphic computing, which mimics the structure and behavior of the human brain. Neuromorphic circuits, designed with low-power consumption in mind, offer a promising direction for future computing systems, especially in applications related to artificial intelligence and machine learning.

Additionally, the continued evolution of 3D integrated circuits (ICs) holds promise for reducing power consumption in VLSI circuits by enabling more efficient interconnection of circuit layers and reducing the physical distance between components. The integration of multiple layers could also help mitigate heat dissipation issues, further improving energy efficiency.

5. FUTURE WORK

Future research in low-power VLSI design should focus on integrating emerging technologies like AI-driven optimization, neuromorphic computing, and 3D ICs to enhance power efficiency while maintaining high performance. AI can automate power optimization, enabling adaptive systems that adjust to varying workloads, while neuromorphic computing and 3D ICs offer exciting possibilities for reducing power consumption in complex systems. Additionally, exploring energy harvesting techniques, quantum computing, and advanced materials like graphene could lead to more sustainable and efficient circuits. Optimizing power-performance trade-offs and developing hybrid architectures will also be crucial to meet the evolving demands of next-generation computing.

6. CONCLUSIONS

the design and optimization of low-power VLSI circuits for next-generation computing is a critical and rapidly evolving field, with significant implications for various industries, including mobile computing, IoT, and artificial intelligence. This research has explored several key techniques for power optimization, such as clock gating, power gating, dynamic voltage scaling, and multi-threshold CMOS. Through a comprehensive analysis of trade-offs between power, performance, and area, it has become clear that achieving the optimal balance between these factors remains a challenge, especially as demand for higher performance increases.

The findings of this study highlight the effectiveness of low-power design techniques in improving energy efficiency without compromising computational speed or area. However, the study also underscores the need for continued innovation in circuit design and technology to address ongoing challenges, such as the integration of emerging materials, the

application of machine learning algorithms, and the development of more advanced power management strategies.

Looking ahead, the future of low-power VLSI design will likely be shaped by advancements in AI, neuromorphic computing, and 3D ICs, all of which have the potential to revolutionize the way circuits are designed and optimized. As computational demands continue to grow, further research into these areas will be essential to ensure that the power efficiency of next-generation systems keeps pace with their increasing complexity. In conclusion, the ongoing evolution of low-power VLSI design holds great promise for enabling more sustainable and efficient computing solutions in the years to come.

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8. AUTHOR CONTRIBUTIONS

1. A.T.M. TariqulAlam: Conceptualization, Methodology, Simulation, Writing – Original Draft.
2. Md.Foridul Hassan: Formal Analysis, Investigation, Data Curation, Writing – Review & Editing.
3. Sadia Afrin: Validation, Visualization, Literature Review, Writing – Review & Editing.

All authors have read and approved the final manuscript.

9. DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

10. FUNDING

This research received no external funding.

11. ETHICAL APPROVAL

This article does not contain any studies with human participants or animals performed by any of the authors.

12. CONFLICT OF INTEREST

The authors declare that there is no conflict of interest regarding the publication of this paper.

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