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Comparative Analysis of 4-bit Low-power Encoders for 1 GS/s in 90 nm CMOS Technology

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ABSTRACT

The meticulous design and optimization of the encoder is essential to achieve a high-performance in flash ADCs suitable which are used for high-speed applications. The encoder in a flash ADC is critical circuit because it translates the raw output from the comparators. The performance of a encoder affects the accuracy, speed, resolution, and overall quality of the ADC's output and making it a pivotal circuit in the analog-to-digital conversion process. Three methods of encoders have been simulated that are pseudo-dynamic CMOS encoders, priority encoders, and MUX-based encoders at a sampling frequency of 1 GHz with a supply voltage of 0.8 V. According to the comparison, the MUX-based encoders have significant advantages and challenges when compared to priority and pseudo-dynamic CMOS encoder architectures. The MUX-based encoder provides increased flexibility, improved scalability, and easier implementation across a variety of input configurations, allowing for more flexible digital circuit designs with minimal added logic complexity. It is also suitable for designing ADCs for low-power applications. The total power consumption of a 4-bit priority encoder is 25.36 µW. The total power consumption of a 4-bit pseudo-dynamic CMOS encoder is 41.76 µW. The power consumption of the 4-bit MUX-based encoder is 20.57 µW. From the simulation results, the MUX-based encoder circuit uses less power than the pseudo-dynamic CMOS encoder and priority encoder. The active area of the MUX-based encoder is 53.4 µm* 30.8 µm.

Keywords

Flash ADC, Thermometer code, Priority, Pseudo, Multiplexer, Encoder

1. INTRODUCTION

Encoders serve an important role in translating thermometer code to binary output [1], [2]. These encoders are essential components that have a considerable impact on the overall performance of ADC [3], [4]. Several types of encoders are described in the literature, they differ in circuit complexity, power consumption and sampling rate. The implementation ROM-based encoder has a simple approach, high operating reliability, and suitable for low-speed applications. However, the large area results in significant power dissipation and limited speed due to access time [5]. Priority encoders have a simple logical structure, highly reliability, and easy to implement. Speed constraints owing to priority chain, higher power consumption in active state and limited scalability for high resolutions are the some of the limitations [6], [7]. A pseudo-CMOS encoder has good power efficiency, high-speed operation capability, and a compact architecture. But complex in the design requirements, sensitive to process variations, and the design cost is higher [8]. MUX-based encoders provide faster performance, parallel processing capabilities, scalability, and a versatile architecture. Static and dynamic power consumption is less due use of static CMOS design [9] - [14]. Wallace tree encoders are capable of providing a high-speed operation, efficient parallel processing, as the result it is suitable for high-resolution ADCs. but the circuit implementation is complex and consumes high power [15], [16]. Fat tree encoder provides an improved performance leads to higher which is ideal for medium to high-resolution. However, it is occupied larger space compared to simple encoders, and higher power consumption [17], [18]. Among the encoder types, pseudo-CMOS is optimum for power-constrained designs, modified priority encoder for medium-speed requirements, MUX-based design for power optimisation techniques, and all three preferred for low-power applications [19]. This study compares only three types of encoders: MUX-based encoder, priority encoder, and pseudo-dynamic CMOS encoder. All the simulations were carried out using Cadence Virtuoso in 90 nm CMOS technology. The remaining part of the paper is arranged as follows. Section II discusses three types of encoders: priority, pseudo-dynamic CMOS, and MUX-based. The simulation and results are discussed in Section III. The conclusion is stated in section IV.

2. STUDY OF ENCODERS

An encoder is a combinational logic circuit that receives 2^N input lines and generates N output lines. Thermometer code can be converted to binary code using various kinds of techniques, including a MUX-based encoder, a pseudo-dynamic CMOS encoder, and a priority encoder. Priority, pseudo-dynamic CMOS, and MUX-based encoders are meticulously designed for 4-bit operation in 90 nm CMOS technology. The power and delay characteristics are analysed in order to identify the most energy-efficient encoder for flash ADC architecture. The advantages and disadvantages of each of these encoders are discussed.

2.1 Priority Encoder

In the case of an ordinary encoder, one and only one decimal input can be activated at any given time. But in the case of some practical digital systems, two or more decimal inputs can unintentionally become active at the same time, which might cause confusion. This kind of problem can be solved with the help of a priority encoder [6]. Priority encoders have several inputs that are routinely active at the same time. In such cases, the primary function of the encoder is to select the input with the highest priority. This function of the priority encoder is known as arbitration.

2.1.1 4-Bit Priority Encoder. Priority encoders are essential components of modern digital circuits, which are frequently used in the areas of data compression, data matching, and network routing. The 4-bit priority encoder circuit consists of 16 input lines (D15 to D0) and 4 output lines (Q3, Q2, Q1, and Q0), and the truth table for the same is given in Table 1. The encoder generates the binary code that corresponds to the input with the highest priority, if there are multiple inputs with logic high. It uses the location of the highest priority active input to generate the output binary code. The output code is often zero or a default state if there are no active inputs (all the inputs are 0's) present. The output of the 4-bit priority encoder

Table 1. Truth table of 4-bit priority encoder

Input D15 to D0•	Output Q3 to Q0•
0000000000000000	xxxx
0000000000000001	0000
000000000000001x	0001
00000000000001xx	0010
0000000000001xxx	0011
000000000001xxxx	0100
00000000001xxxxx	0101
0000000001xxxxxx	0110
000000001xxxxxxx	0111
00000001xxxxxxxx	1000
0000001xxxxxxxxx	1001
000001xxxxxxxxxx	1010
00001xxxxxxxxxx	1011
0001xxxxxxxxxxx	1100
001xxxxxxxxxxxx	1101
01xxxxxxxxxxxxx	1110
1xxxxxxxxxxxxxx	1111

will be determined by logical combinations of the 16 inputs. Q_3 will be 1 if any of the inputs in groups D_1, D_3, D_5, D_9, D_{11}, D_{13}, D_{15} are active and the same is expressed in "Eq. (1). Q_2 will be 1 if any of the inputs in groups D_2-D_3, D_6-D_7, D_{10}-D_{11}, D_{14}-D_{15} are active as given in "Eq. (2). Q_1 will be 1 if any of the inputs from D_4 to D_7 or D_{12} to D_{15} are active as provided in "Eq. (3). Similarly, Q_0 will be 1 if any of the inputs from D_8 to D_{15} are active is given in "Eq. (4).

$$Q0 = D_8 + D_9 + D_{10} + D_{11} + D_{12} + D_{13} + D_{14} + D_{15} \quad (1)$$

$$Q1 = D_4 + D_5 + D_6 + D_7 + D_{12} + D_{13} + D_{14} + D_{15} \quad (2)$$

$$Q2 = D_2 + D_3 + D_6 + D_7 + D_{10} + D_{11} + D_{14} + D_{15} \quad (3)$$

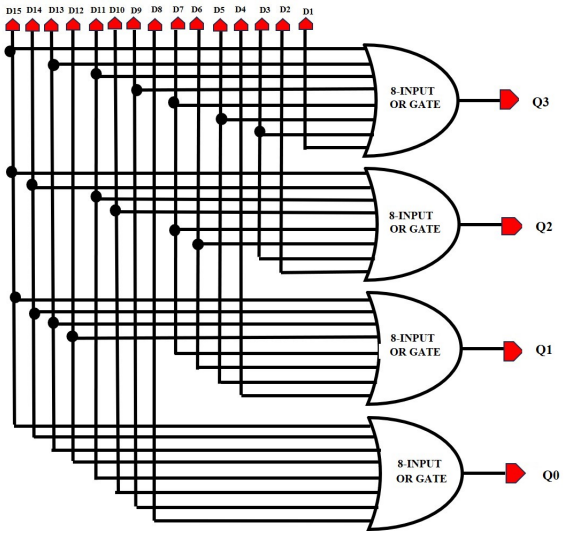

Fig. 1. Circuit diagram of 16:4 priority encoder using 8-input OR gate.

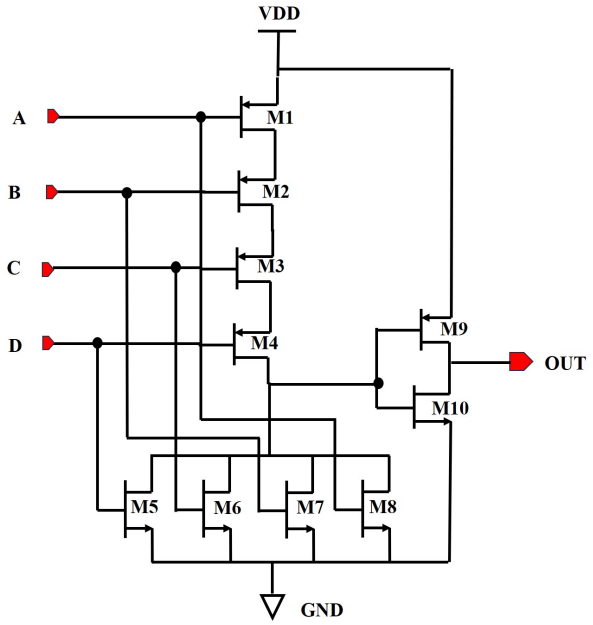

Fig. 2. Circuit diagram of 8-input OR gate.

$$Q3 = D_1 + D_3 + D_5 + D_7 + D_9 + D_{11} + D_{13} + D_{15} \quad (4)$$

The 4-bit priority encoder design requires four 8-input OR gates shown in Figure 1. Seven 2-input OR gates are needed for an 8-input OR gate is given in Figure 2. The schematic diagram for the 2-input OR gate circuit is shown in Figure 3. The 8-input OR gate is used in the priority encoder design. Compared to multiple smaller gates connected in series, an 8-input OR gate processes the signals faster. This is because carrying out the logic operation in a single stage reduces the propagation time.

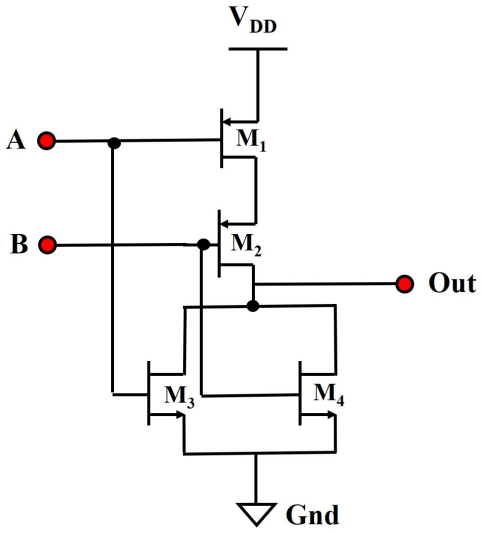

Fig. 3. Circuit diagram of 2-input OR gate.

2.2 Pseudo-Dynamic CMOS logic

Pseudo dynamic CMOS encoder includes dynamic CMOS and static CMOS devices. The pseudo-dynamic CMOS logic makes use of OR and AND logic gates, identical to the PLA design. This architecture only uses specific input combinations in order to produce an output, unlike PLA, which combines all inputs to produce an output bit [8]. A pseudo-dynamic CMOS logic circuit consists of an inverter, a group of NMOS transistors in a pull-down network, and a PMOS transistor in the pull-up network with a gate connected to the clock as shown in Figure 4.

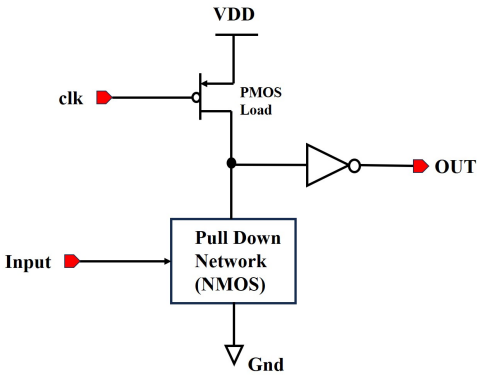

Fig. 4. Circuit diagram of pseudo-dynamic CMOS logic.

2.2.1 4-Bit Pseudo-Dynamic CMOS Encoder. Pseudo-dynamic CMOS logic design is better than other logic designs for high-speed flash ADC architecture because of its lower transistor count. It has advantages of reduced critical path latency and moderate power dissipation. The main advantage of the pseudo-dynamic CMOS encoder is that it converts thermometer code to binary code directly, without any intermediate conversions. For a 4-bit pseudo-dynamic CMOS encoder, the generation of output bits is bit3, bit2, bit1, and bit0, which are given in "Eq. (5), "Eq. (6), "Eq. (7), and "Eq. (8)

$$bit3 = i_7 \tag{5}$$

$$bit2 = i_0\bar{i_3} + i_1 \tag{6}$$

$$bit1 = i_1\bar{i_3} + i_5\bar{i_7} + i_9\bar{i_{11}} + i_{13} \tag{7}$$

$$bit0 = i_0\bar{i_1} + i_2\bar{i_3} + i_4\bar{i_5} + i_6\bar{i_7} + i_8\bar{i_9} + i_{10}\bar{i_{11}} + i_{12}\bar{i_{13}} + i_{14} \tag{8}$$

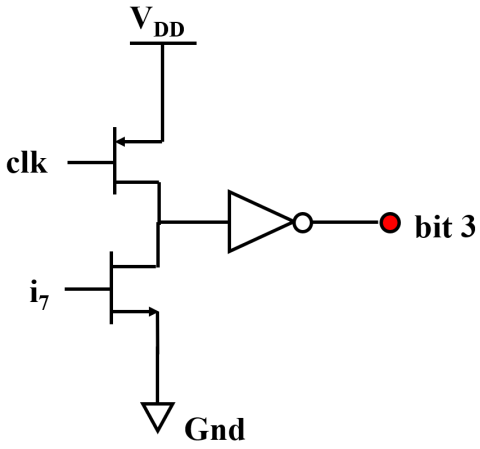

Fig. 5. Circuit diagram of generation bit 3 of pseudo-dynamic CMOS encoder.

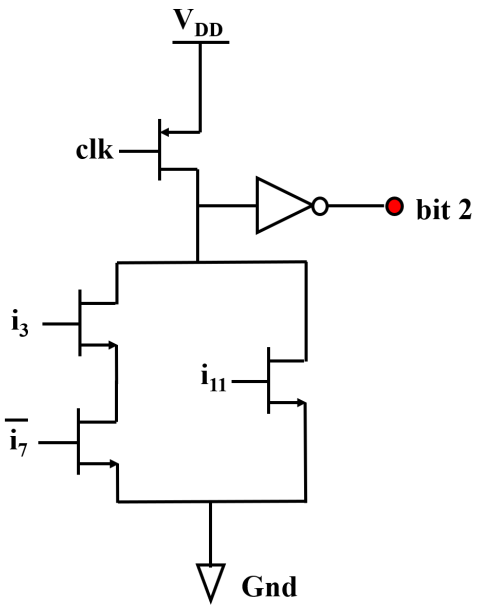

Fig. 6. Circuit diagram of generation bit 2 pseudo-dynamic CMOS encoder.

The generation of bit3 is equated to input i7, as shown in Figure 5. The generation of bit2 is the input combination i_0, i_1, $\bar{i_3}$ is shown in Figure 6. The generation of bit1 is the input combination i_1, $\bar{i_3}$, i_5, $\bar{i_7}$, $\bar{i_{11}}$ and i_{13} is shown in Figure 7. Similarly, the generation of bit0 is the input combination i_0, $\bar{i_1}$, i_2, $\bar{i_3}$, i_4, $\bar{i_5}$, i_6, $\bar{i_7}$, i_8, $\bar{i_9}$, i_{10}, $\bar{i_{11}}$, i_{12}, $\bar{i_{13}}$, and i_{14} are displayed in Figure 8.
In pseudo-dynamic CMOS logic, the NMOS evaluation logic can be enabled during the pre-charge phase as it has no influence on the output voltage due to the presence of the inverter. It is necessary to make sure that the voltage at the inverter input does not exceed V_{IH}, which is the maximum input voltage that the inverter considers as logic zero. The PMOS and NMOS transistor sizes must be carefully set in order to do this; otherwise, the logic circuit would not perform as desired. Dynamic node pre-charging is a common

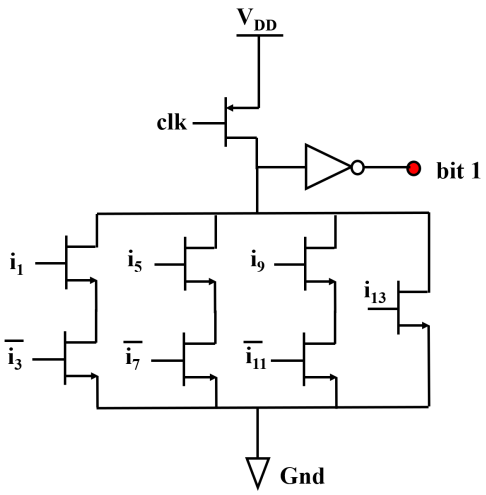

Fig. 7. Circuit diagram of generation bit 1 pseudo-dynamic CMOS encoder.

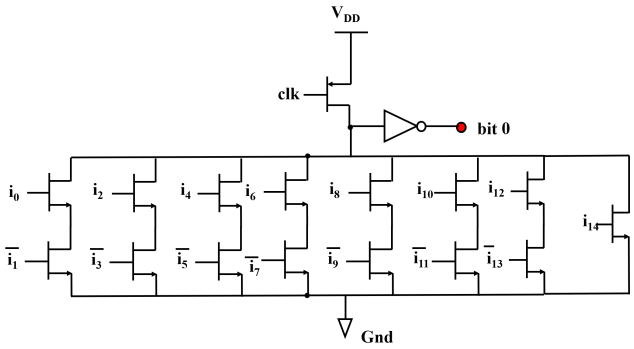

Fig. 8. Circuit diagram of generation bit 0 pseudo-dynamic CMOS encoder.

feature of pseudo-dynamic CMOS logic. During the pre-charging phase, a timed pre-charge transistor charges the dynamic nodes to a predetermined voltage level, readying them for the next input signal. During the evaluation phase, a pull-down network of transistors may allow the dynamic nodes to discharge, depending on the input signals. The logic evaluation to get the desired output is demonstrated by this transistor discharge. Through charge-sharing and discharge of the dynamic nodes, the circuit transmits signals that provide the required encoding.

2.3 MUX-Based Encoder

A multiplexer is a combinational circuit that has many data inputs and a single output. The output is produced depending on control or select inputs [9]. For 2^n input lines, n selection lines are needed. Multiplexers are also known as "N-to-1 selectors," parallel-to-serial converters, many-to-one circuits, and universal logic circuits.

2.3.1 2:1 Multiplexer. The 2:1 Multiplexer (MUX) is a fundamental circuit that are used to choose one signal from two inputs and transmits it to the output. The 2:1 MUX has two input lines, one output line, and a single selection line, as shown in Figure 9, where I_0 and I_1 are the input lines, and Y is the output line, and S_0 is a single select line. The output of the 2:1 MUX will depend on the selection line S_0. When S_0 is 0 (low), input I_0 is selected; when S_0 is 1 (high), input I_1 is selected. The logical expression for the

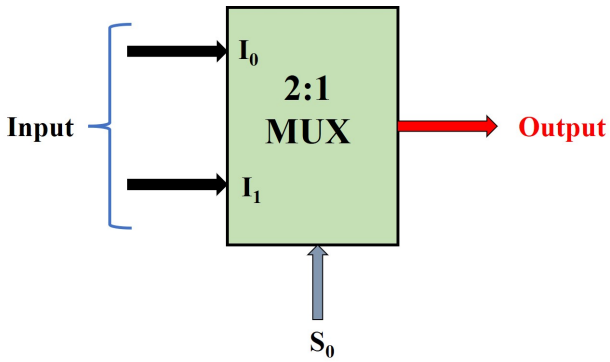

Fig. 9. Block diagram of 2 to 1 Multiplexer.

Table 2. Truth table of 2:1 MUX

S_0	I_0	I_1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

2:1 MUX can be determined from Table 2 as in "Eq. (9)

$$Y = (\bar{S_0})I_0 + (S_0)I_1 \tag{9}$$

2.3.2 4-Bit MUX-Based Encoder. The MUX-based encoder is useful for circuits with lower power consumption since it has a short critical path, requires less hardware, and maintains a lower bubble error. The 4-bit MUX-based encoder combines multiple input signals into a binary code, the basic idea is to select the active input using a collection of 2:1 MUX, and generate the binary code in accordance with the input selection. MUX-based encoding is implemented using a binary search approach, and the truth table for

the same is given in Table 3. The circuit diagram of a 2-input

Table 3. Truth table of 4-bit MUX-based encoder

Input D15 to D0•	Output Q3 to Q0•
0000000000000000	XXXX
0000000000000001	0000
0000000000000010	0001
0000000000000100	0010
0000000000001000	0011
0000000000010000	0100
0000000000100000	0101
0000000001000000	0110
0000000010000000	0111
0000000100000000	1000
0000001000000000	1001
0000010000000000	1010
0000100000000000	1011
0001000000000000	1100
0010000000000000	1101
0100000000000000	1110
1000000000000000	1111

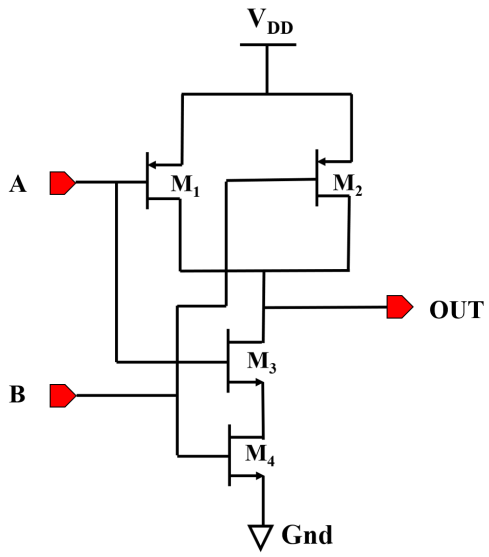

Fig. 10. Circuit diagram of 2-input NAND gate.

NAND gate is shown in Figure 10. The schematic diagram of the 2:1 MUX is shown in Figure 11. To design a 2:1 MUX, four 2-input NAND gates are required. The circuit diagram of a 16:4 MUX-based encoder is shown in Figure 12. The MUX-based encoder has eleven 2:1 MUXs. Furthermore, 44 NAND gates are required in total for designing a 16:4 MUX-based encoder. A 2:1 MUX that chooses one of two input data lines and directs it to the output. The selection is controlled by a single ”select” or ”control” line. There is a single select line (S) that determines which of the two input

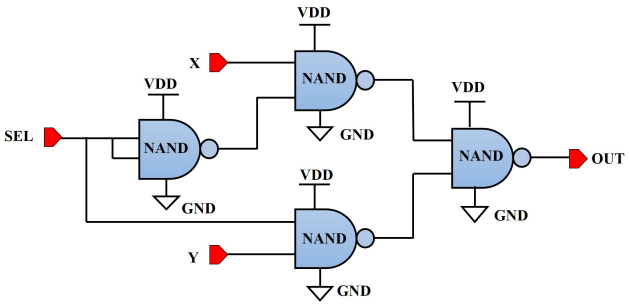

Fig. 11. Circuit diagram of 2:1 MUX using NAND gate.

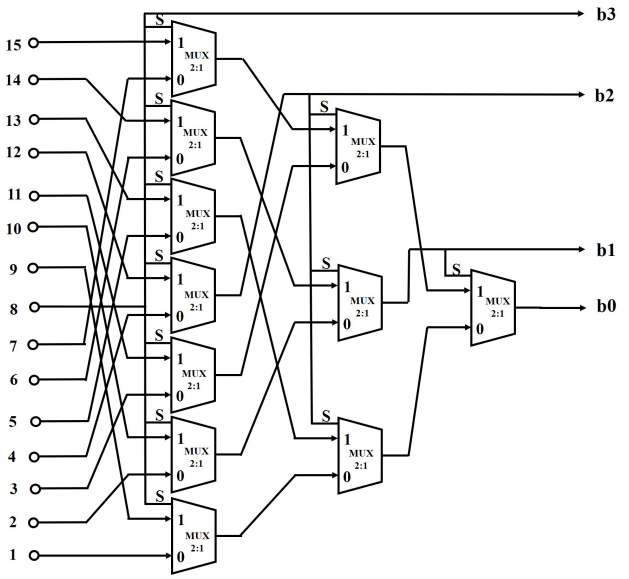

Fig. 12. Circuit diagram of 16:4 MUX-based encoder.

lines is transmitted to the output. As MUX-based encoders have fewer hardware and a shorter critical path, they are more suited for circuits with lower power consumption.

3. RESULTS AND DISCUSSION

The design of three different encoder circuits is considered, and their performance is analysed through a simulation study in terms of delay and power consumption. The performance of these encoders is compared to each other at a supply voltage of 0.8 V and a clock frequency of 1 GHz in 90 nm technology. The transient response of a 2-input OR gate is studied from 0 to 5 ns, and the same is shown in Figure 13. The output of an OR gate goes to high when any one of the inputs is high. The power consumption of a 2-input OR gate is 905.885 nW. The transient response of the 8-input OR gate for the given input (D0 - D3) is considered starting from 0 to 8 ns as given in Figure 14. For the given input (D4 - D8), the output transient response is shown in Figure 15. The power consumption of the 8-input OR gate is found to be 6.34 µW. The transient response of the 4-bit priority encoder for a time range of 0 to 8 ns is analysed as shown in Figure 16. The priority encoder requires a total of 168 transistors, and it consumes a total of 25.36

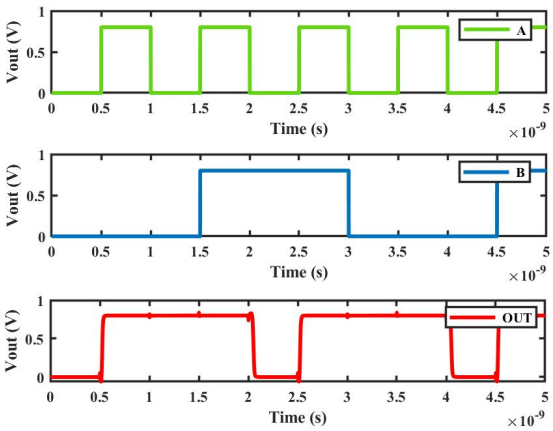

Fig. 13. Transient response of 2-input OR gate.

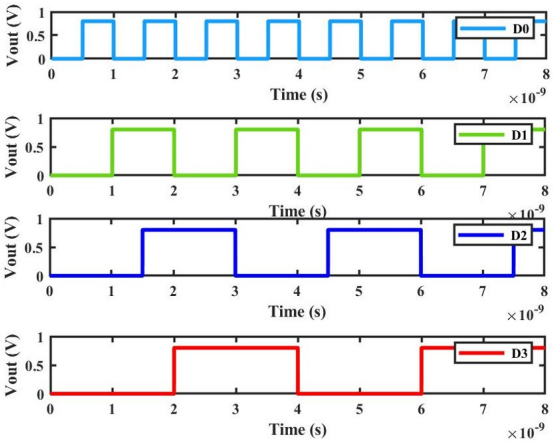

Fig. 14. Input waveform 8-input OR gate (D0 t0 D3).

µW of power when sampling at 1 GHz. The worst-case latency is 0.5 ns. To design a 4-bit pseudo-dynamic CMOS encoder, 41 transistors are required. Dynamic node pre-charging is a common characteristic of pseudo-dynamic CMOS logic. During the pre-charge phase, the nodes are pre-charged to a specific voltage. The output code is generated using the combination of the selected inputs. The power consumption of bit0, bit1, bit2, and bit3 for the pseudo-dynamic CMOS encoder is 15.22 µ W, 11.36 µW, 8.313 µW, and 6.87 µW, respectively. The overall power consumption of a 4-bit pseudo-dynamic CMOS encoder is 41.76 µW. The worst-case delay is 3.55 ns. The design of a 4-bit MUX-based encoder requires 176 transistors. In order to design a 16:4 MUX-based encoder, 11 MUXs are needed, and 4 NAND gates are required to implement a 2:1 MUX. The transient response of a 2-input NAND gate is shown in Figure 17. The power consumption of a 2-input NAND gate is found to be 430.7 nW. Output response of 2:1 MUX is given in Figure 18. The total power consumption of the 2:1 MUX is 1.87 µW. The transient response of the 4-bit MUX-based encoder is shown in Figure 19. The total power consumption is 20.57 µW at a sampling

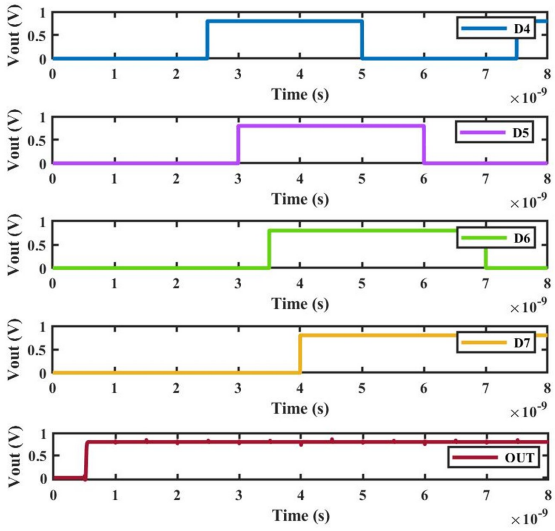

Fig. 15. Input waveform and output response of 8-input OR gate (D4 to D8,output respose).

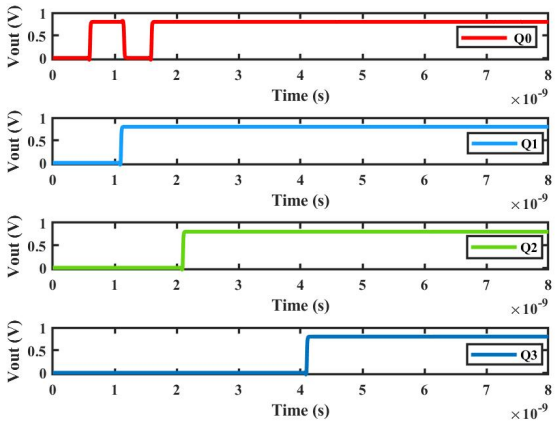

Fig. 16. Transient response of 4-bit priority encoder.

frequency of 1 GHz. The worst-case delay is 7.0 ns. A 4-bit MUX-based encoder has been chosen for the flash ADC implementation because of its benefits over the other encoders. After the design and analysis, the pre-layout and post-layout of the 2-input NAND gate are considered to verify the mismatches and the effect of parasitic components on its performance. The active area of a 2-input NAND gate is 3 µm* 3.3 µm*.

The power consumption of the NAND gate is 431.7 nW after the post-layout. The pre-layout and post-layout of the 2:1 MUX are shown in Figure 20 (a) and Figure 20 (b). The active area of the 2:1 MUX is 8.15 µm* 10.14 µm. The power consumption of the 2:1 MUX is 2.13 µW after the post-layout. Finally, the pre-layout and post-layout of the 4-bit MUX-based encoder are shown in Figure 21 (a) and Figure 21 (b). The active area of the 4-bit MUX-based encoder is 53.4 µm* 30.8 µm.

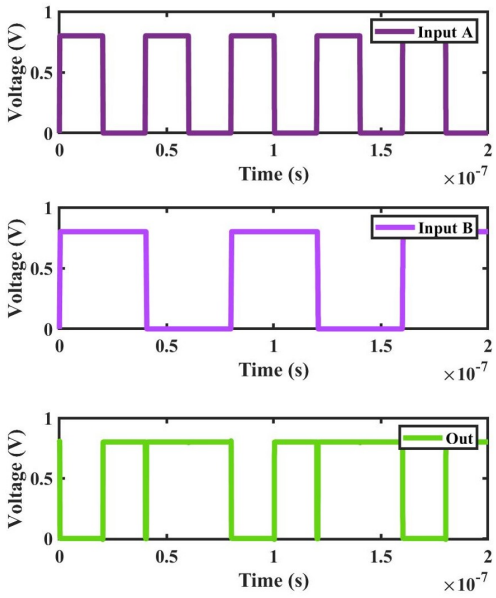

Fig. 17. Transient response of 2-input NAND gate.

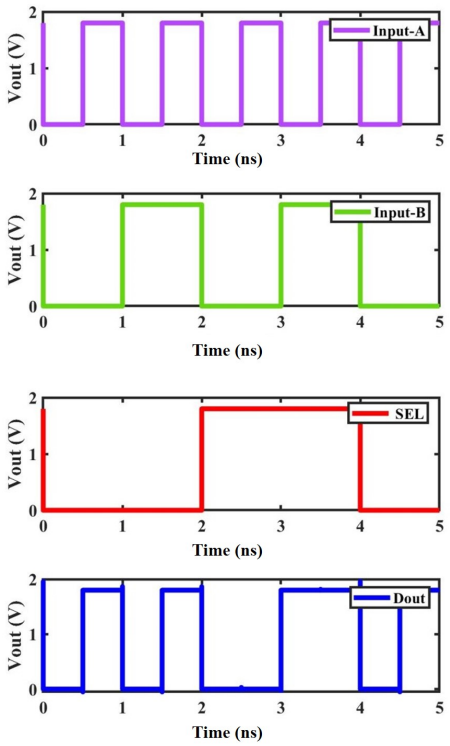

Fig. 18. Transient response of 2:1 MUX.

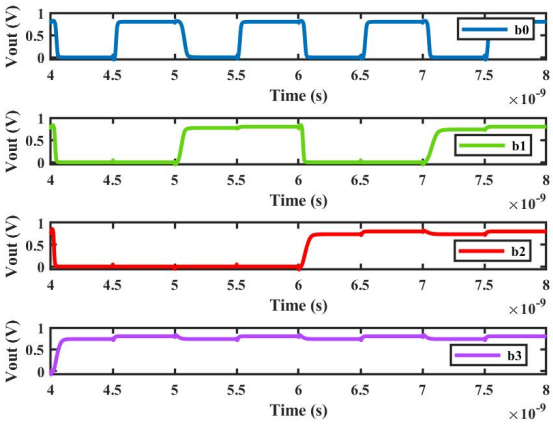

Fig. 19. Transient response of 4-bit MUX-based encoder.

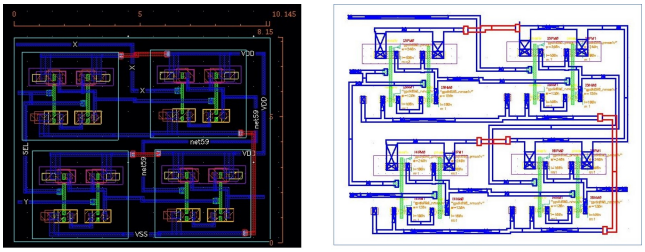

Fig. 20. Layout of 2:1 MUX : (a) pre-layout (b) post-layout.

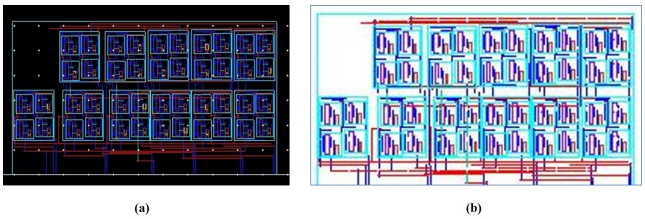

Fig. 21. Layout 4-bit MUX-based encoder : (a) pre-layout (b) post-layout.

4. SUMMARY

Three encoder architectures Pseudo, Priority, and Mux-based—implemented using identical design parameters of 90 nm technology, 0.8 supply voltage, and 1 GHz sampling frequency are compared comprehensively in Table 4. The simulation results reveal distinct trade-offs between power consumption and delay in terms of performance. The Dynamic Priority encoder, which is approximately 7.1 times faster than the pseudo encoder (3.55 ns) and 14 times faster than the Mux-based encoder (7.0 ns), exhibits excellent speed performance with the lowest delay of 0.5 ns. however, the Mux-based encoder performs extremely well in terms of power consumption, using the least amount of power (20.57 µW), saving 50.7% over the Pseudo encoder (41.76 µW) and 18.9% over the Dynamic Priority encoder (25.36 µW).

The Mux-based encoder is better suited for power-constrained systems where energy efficiency takes precedence over speed, the Dynamic Priority encoder is the best option for speed-critical applications where minimising propagation delay is crucial. The power consumption of the 4-bit MUX-based encoder is 21.62 µW. **The graph illustrates a clear inverse relationship between delay and power performance across the three designs is shown in Figure 22. Mux-based saves 50.7 % power vs Pseudo encoder also, Mux-based saves 18.9 % power vs Priority encoder.** From the results, it is found that the MUX-based encoder consumes less power in comparison to the other two encoders.

Table 4. Simulation results comparison of three different encoders

Parameters	Pseudo Dynamic	Priority	Mux-based
Technology (nm)	90	90	90
Supply voltage (V)	0.8	0.8	0.8
Sampling frequency (Hz)	1 G	1 G	1 G
Delay (ns)	3.55	0.5	7.0
Total power µW	41.76	25.36	20.57

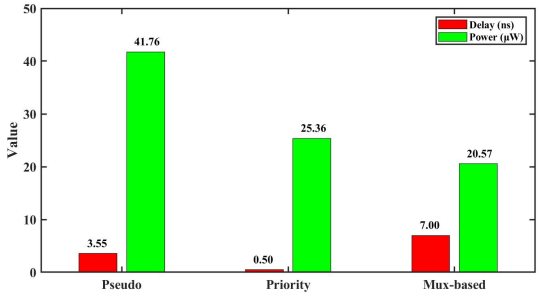

Fig. 22. Comparative analysis of delay and power.

5. CONCLUSION

In this paper, different types of encoders are considered for the flash ADC implementation, such as pseudo-dynamic CMOS, priority, and MUX-based encoders, and the performance for the same is analysed through a simulation study with a supply voltage of 0.8 V at a sampling frequency of 1 GHz in 90 nm CMOS technology. The priority encoder circuit gets more complicated as the number of inputs increases in comparison to other circuits. When the input data width is large, a high-performance priority encoder is required; nevertheless, it has limitations such as excessive delay and high-power consumption. In comparison to conventional encoder designs, the pseudo-dynamic CMOS encoder's inherent speed limitations and increased circuit complexity impair its effectiveness in high-frequency applications. There are significant benefits as well as limitations to MUX-based encoders when compared to priority and pseudo-dynamic CMOS encoder designs. This provides improved scalability, increased flexibility, and easier implementation across a variety of input combinations, allowing for more flexible digital circuit designs with less extra logic complexity. Additionally, MUX-based encoders offer improved signal handling capabilities. It is also suitable for designing ADCs for low-power applications. **Future work can focus on improving the power efficiency and scalability of MUX-based encoders by integrating a novel transistor-level optimization method.**

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