A Comprehensive Survey on SmartNIC

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ABSTRACT
This survey paper provides a comprehensive overview of Smart Network Interface Cards (SmartNICs) with a focus on their classification based on application, benchmark, and hardware implementation. The study explores the diverse range of applications where SmartNICs are utilized, including data flow, storage, networking, and offloading. It explores the various benchmarks used to evaluate the performance of SmartNICs, such as throughput, latency, and packet processing capabilities. The paper discusses the different hardware implementations of SmartNICs, including FPGA-based SmartNICs. By examining these classifications, this survey aims to provide insights into the developing landscape of SmartNIC technology and its impact in distributed computing.

Keywords
Distributed computing, SmartNIC, offloading, FPGA SmartNIC.

1. INTRODUCTION
In this investigation, our focus lies on the industrial and scholarly exploration of heterogeneous computing utilizing a novel category of computing apparatus recognized as data processing unit. Just as network interface cards (NIC) spurred the creation of intelligent network interface cards (SmartNIC), we are witnessing analogous progressions in the realm of SmartNICs. Recent advancements in SmartNICs by prominent companies such as Nvidia and AMD have ushered in a new epoch of smartNIC. An important characteristic of a SmartNIC is its incorporation of a general-purpose CPU capable of executing an operating system within a conventional SmartNIC, albeit with CPU cores of lesser potency compared to the host's CPU cores. This examination centers on the utilization of smartNIC, its technology for hardware integration and evaluation, investigating its repercussions on system architecture and network efficiency. We delve into how SmartNICs not only alleviate the computational load on the host CPU by delegating tasks but also boost system effectiveness and scalability. Additionally, we scrutinize the role of SmartNICs in expediting the fusion of storage, computation, and networking responsibilities into a unified system, a vital aspect in contemporary data-intensive applications necessitating high throughput and minimal latency.

Our scrutiny expands to the diverse architectural configurations of SmartNICs and how various producers are harnessing this technology to expand the frontiers of data processing capabilities. By executing intricate processing activities directly at the network periphery, SmartNICs empower more flexible and astute management of data streams, considerably diminishing data congestion and enhancing overall network flexibility.

This delivers a discerning assessment of the present state of SmartNIC technology, encompassing its applications, advantages, and hurdles. We culminate with a discourse on the forthcoming trends and potential research trajectories in this swiftly evolving domain, accentuating the transformative capacity of SmartNICs in the forthcoming era of distributed computing systems.

2. WHAT IS SMARTNIC
A SmartNIC - Smart Network Interface Card, is a specialized type of network interface card that can execute tasks that go beyond the conventional functions of networking. These tasks may include, but are not limited to, the offloading of processing from the central processing unit (CPU), strengthening security measures, and expediting network functions. SmartNICs such as BlockNIC and the AMD 400-G Adaptive SmartNIC reduces the utilization of CPU and hardware within data centers by facilitating direct computation on the network itself. This innovative technology enables the efficient operation of blockchain infrastructure, enhances the performance of virtual network devices using Field-Programmable Gate Array (FPGA) accelerators, and ensures expedited acceleration for cloud-based network and storage applications. The distinctive characteristics of these SmartNICs encompass programmable logic, hardware acceleration capabilities, and security components like cryptographic acceleration, all of which are strategically integrated to elevate the efficiency and security of data processing operations.

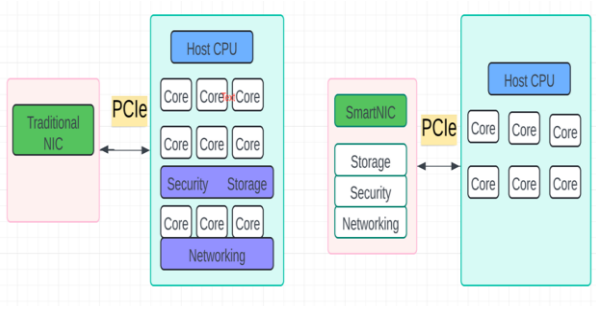

Fig 1: Computational architecture of SmartNIC [2,6,7]

3. SUMMARY OF PAPERS
Jiaxin Lin et al. [1] present 'PANIC', a programmable NIC capable of diverse offloads connected through a non-blocking switching fabric. It is a novel approach since existing NICs either offer only specific types of offloads or lack flexibility in offload chaining and multi-tenant isolation. Experimental results from a 100 Gbps FPGA-based prototype show that this design can overcome the limitations of state-of-the-art programmable NICs. The architecture of PANIC enables efficient routing of packets through three units in just 0.5 microseconds, demonstrating its ability to maintain low latency while handling various packet sizes sequentially.

Zerui Guo et al. [2] present 'LogNIC', a high-level performance model designed for SmartNICs. It is a specialized network card that accelerates data processing in data centers by offloading computational tasks from CPUs or servers. Experimental results show that this model can improve

application performance by up to 36.4% and reduce delay by 22.8% compared to older methods.

Zerui Guo et al. [3] introduce 'LEED', a novel method for fast and energy-efficient data storage and retrieval on SmartNIC JBOFs. This model outperforms existing solutions in both speed and power efficiency when handling small to medium-sized data, achieving a 4.2×/3.8× and 17.5×/19.1× improvement in energy efficiency over traditional server storage and smaller embedded storage nodes, respectively.

Marco et al. [4] present 'hXDP', an innovative compiler optimization approach that translates and parallelizes eBPF bytecode—a soft CPU—for execution on FPGAs. The infrastructure supports XDP maps and helper functions, enhancing packet processing throughput and reducing latency. Using only 15% of FPGA resources, hXDP efficiently runs Linux's XDP programs on FPGA NICs.

Ming Liu et al. [5] introduce 'Floem', a framework for developing server programs that utilize NIC accelerators. It includes a language, compiler, and runtime system to help developers delegate tasks to hardware, manage data flow, and optimize communication between the CPU and NIC without complex programming. When tested on a key-value store and a real-time analytics system, Floem improved throughput by 1.3–3.6× and 75–96%, respectively, compared to CPU-only solutions.

Jiaxin Lin et al. [6] introduce 'Ringleader', a system that shifts request management from the server's main CPU to the NIC, enhancing response time and resource efficiency. A 100 Gbps FPGA-based prototype demonstrated superior scalability, latency, throughput, and efficiency compared to leading software-only orchestrators such as Shinjuku and Caladan.

Zeke Wang et al. [7] present 'FpgaNIC', a GPU-centric SmartNIC that enables direct data communication between GPUs and the network, minimizing CPU involvement. It is the first FPGA-based SmartNIC tailored for GPU applications and supports 100 Gbps network traffic. Experimental results indicate that FpgaNIC can handle up to 1000 Gbps traffic, a substantial improvement over existing SmartNICs.

Kaushik Kandadi et al. [8] propose a framework for offloading any type of communication operation to NVIDIA's BlueField DPUs. This reduces host CPU workload and boosts communication efficiency without being constrained to specific algorithms or patterns. The framework shows up to 47% improvement in Alltoall micro-benchmarks and notable application-level improvements, including up to 60% in P3DFFT and 15% in HPL on 512 processes.

Boris Pismenny et al. [9] introduce 'Autonomous NIC Offloads', which allow NICs to process Layer-5 protocols (e.g., HTTPS and NVMe-over-TCP) independently, without fully offloading the TCP/IP stack. This approach simplifies network data processing, increases throughput by up to 3.3×, and reduces CPU usage and latency by up to 40% and 70%, respectively.

Haggi Eran et al. [10] present 'FlexDriver', a system that allows hardware and FPGA accelerators to control NICs directly, eliminating CPU dependency. It leverages existing NIC features—like virtualization, tunneling, and RDMA—enabling accelerators to perform advanced network tasks. Prototypes on NVIDIA Innova-2 FPGA SmartNICs demonstrated high speeds (25 Gbps) and efficient operations without CPU involvement.

Yan Mu et al. [11] propose a SmartNIC-based offloading framework for Storage Pooling (SOSP), which reduces CPU workload in data centers by offloading both local and remote storage services to SmartNICs. It improves I/O random read/write performance by approximately 20–25% and 13–15%, respectively. Additionally, it frees up to 16.7% of host CPU resources, enhancing computational capacity for other services.

Jianshen Liu et al. [12] demonstrate the use of 'Apache Arrow' as a foundational technology for executing data-flow tasks on SmartNICs. Experiments show that deploying Apache Arrow on the BlueField-2 SmartNIC significantly accelerates particle data processing by leveraging the NIC's hardware compression and decompression capabilities.

4. CLASSIFICATION BASED ON THE APPLICATION OF SMARTNIC

Table 1. Classification based on the application of SmartNIC

Title	Data flow	Network	Storage	Offload
1. PANIC: A High-Performance Programmable NIC for Multi-tenant Networks	√			
2. LogNIC: A High-Level Performance Model for SmartNICs				√
3. LEED: A Low-Power, Fast Persistent Key-Value Store on SmartNIC JBOFs			√	
4. hXDP: Efficient Software Packet Processing on FPGA NICs		√		
5. Floem: A Programming System for NIC-Accelerated Network Applications				√
6. RingLeader: Efficiently Offloading Intra-Server Orchestration to NICs			√	√
7. FpgaNIC: An FPGA-based Versatile 100Gb SmartNIC for GPUs		√		
8. A novel framework for efficient offloading of communication operation to Bluefield				√
9. Autonomous NIC offload	√			√
10. FlexDrive: A network driver for your accelerator		√		
11. SOSP: A SmartNIC-based offloading framework for cloud storage pooling				√
12. Processing Particle Data flow with SmartNIC	√			√

4.1 Storage

A smartNIC is an essential component in modern data centers, enhancing network performance and security [2]. The storage system of a smartNIC plays a crucial role in optimizing data processing and reducing latency. By efficiently storing and accessing data directly on the SmartNIC, it streamlines operations and enhances overall system efficiency [6]. This innovative approach to storage management ensures that critical data is readily available for processing, contributing to improved network performance and scalability. In this survey, [2, 6] highlight the storage capability of SmartNIC.

4.2 Offloading

The offloading technology of SmartNIC refers to the capability of a SmartNIC to handle specific network-related tasks, such as packet processing, encryption, and virtualization, offloading these tasks from the host CPU [2,5,6]. This helps improve overall network performance, reduce latency, and free up CPU resources for other computations [8,9,11,12]. Studies [2,5,6,8,9,11,12] highlight the offloading aspects of SmartNIC.

4.3 Networking

The network of SmartNICs refers to a system where multiple SmartNICs are interconnected within a network infrastructure [4,7,10]. Each SmartNIC is capable of handling specific network-related tasks, such as packet processing, encryption, and virtualization, offloading these tasks from the host CPU [4,10]. This distributed approach helps optimize network performance, reduce latency, and efficiently utilize CPU

resources for other computations. [4,7,10] underlines the networking aspect of smartNIC.

4.4 Dataflow

In SmartNIC, the dataflow involves the processing of network-related tasks such as packet processing, encryption, and virtualization directly on the SmartNIC itself [1,9]. This offloads these tasks from the host CPU, allowing for optimized network performance, reduced latency, and efficient utilization of CPU resources for other computations [12]. The SmartNICs within the network infrastructure work together to handle and manage the flow of data efficiently, improving overall network performance and responsiveness. [1,9,12] are highlighting the data flow aspect of smartNIC.

5. CLASSIFICATION BASED ON THE BENCHMARK OF SMARTNIC

Table 2. Classification based on the benchmark of SmartNIC

Title	All_to_all	efficiency	latency	speedup	Load balancing	Throughput
1. PANIC: A High-Performance Programmable NIC for Multi-tenant Networks			√	√		√
2. LogNIC: A High-Level Performance Model for SmartNICs			√			√
3. LEED: A Low-Power, Fast Persistent Key-Value Store on SmartNIC JBOFs		√		√		
4. hXDP: Efficient Software Packet Processing on FPGA NICs		√				√
5. Floem: A Programming System for NIC-Accelerated Network Applications				√		√
6. RingLeader: Efficiently Offloading Intra-Server Orchestration to NICs			√			√
7. FpgaNIC: An FPGA-based Versatile 100Gb SmartNIC for GPUs		√	√	√	√	√
8. A novel framework for efficient offloading of communication operation to Bluefield	√		√			
9. Autonomous NIC offload		√	√			√
10. FlexDrive: A network driver for your accelerator		√		√		
11. SOSP: A SmartNIC-based offloading framework for cloud storage pooling		√				
12. Processing Particle Data flow with SmartNIC				√		

Throughput refers to the amount of data that can be processed and transferred by the SmartNIC within a given period of time. SmartNICs are designed to handle high volumes of network traffic efficiently by offloading tasks such as packet processing, encryption, and virtualization from the host CPU [1,2,4,5,6]. The throughput of a SmartNIC can vary depending on factors such as the specific model, network configuration, and workload demands. Overall, SmartNICs are capable of achieving high throughput rates, which contribute to optimized network performance, reduced latency, and improved overall network responsiveness. In this survey, Studies [1,2,4,5,6,7,9] are highlighting the throughput to calculate the benchmark of SmartNIC.

The latency of a SmartNIC refers to the time it takes for data to travel from the source to the destination through the SmartNIC [1,2,6,5]. SmartNICs are designed to minimize latency by offloading tasks such as packet processing and encryption from the host CPU, allowing for faster data processing and transfer. Factors that can affect the latency of a SmartNIC include the specific model, network configuration, and workload demands. Overall, SmartNICs are capable of reducing latency, which leads to improved network responsiveness and performance. In this survey, studies 1,2,6,7,8,9 are highlighting the latency to calculate the benchmark of SmartNIC.

Speedup in SmartNIC is to the increase in data processing and transfer speeds achieved by offloading tasks from the host CPU to SmartNIC [1,3,5,7]. This enhancement in speedup allows for more efficient utilization of CPU resources for other computations. In this survey article, studies [1,3,5,7,10,12] used speed up in order to calculate the benchmark of smartNIC.

Distribution of network traffic across multiple paths or interfaces to optimize resource utilization and prevent bottleneck is called load balancing in SmartNIC [7]. This feature helps in improving network performance, reliability, and scalability by evenly distributing the workload among different network components. Studies [7] used load balancing to calculate the benchmark of SmartNIC. MPI_All-to-all is a collective operation in the MPI allowing processes to send and receive the same amount of data from each other [8]. It's a combination of MPI_Scatter and MPI_Gather, where each process has buffers for both scattering and gathering elements. In this survey article, studies [8] used all-to-all to calculate the benchmark of SmartNIC.

Recent studies have discovered SmartNIC benchmarks in the context of broader domains such as IoT-based smart healthcare [13,14], cloud computing [18, 24], and edge-driven data flow acceleration [20,23], emphasizing the importance of throughput, latency, and energy efficiency in these application areas. Research on machine learning-based intrusion detection [15], antenna optimization for wireless communication [16,17], and digital twin applications [22] supports the growing relevance of SmartNIC performance metrics in emerging 5G and Industry 4.0 systems.

6. CLASSIFICATION BASED ON HARDWARE IMPLEMENTATION OF SMARTNIC

Table 3. Classification based on hardware implementation of SmartNIC

Title	FPGA
1. PANIC: A High-Performance Programmable NIC for Multi-tenant Networks	
2. LogNIC: A High-Level Performance Model for SmartNICs	√
3. LEED: A Low-Power, Fast Persistent Key-Value Store on SmartNIC JBOFs	
4. hXDP: Efficient Software Packet Processing on FPGA NICs	√
5. Floem: A Programming System for NIC-Accelerated Network Applications	
6. RingLeader: Efficiently Offloading Intra-Server Orchestration to NICs	√
7. FpgaNIC: An FPGA-based Versatile 100Gb SmartNIC for GPUs	√
8. A novel framework for efficient offloading of communication operation to bluefield	
9. Autonomous NIC offload	√
10. FlexDrive: A network driver for your accelerator	√
11. SOSP: A SmartNIC-based offloading framework for cloud storage pooling	
12. Processing Particle Data flow with SmartNIC	

FPGA SmartNIC refers to SmartNICs based on Field-Programmable Gate Array technology. FPGA technology allows users to customize hardware acceleration, enabling the offloading of tasks from the host CPU to the SmartNIC for improved performance and efficiency [4,7,10]. This customization capability makes FPGA SmartNICs versatile and adaptable to various networking requirements. Studies [2,4,6,7,9,10] highlight the use of FPGA SmartNICs to achieve enhanced results.

7. CONCLUSION

SmartNICs have emerged as indispensable co-processors alongside CPUs, particularly in the realm of heterogeneous computing. Their significance goes beyond mere replacements, as they play a pivotal role in enhancing performance and efficiency across various fields. While obstacles remain,

ongoing research is poised to address these challenges, paving the way for further advancements and applications in the future.

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