International Journal of Computer Applications (0975 - 8887)
Volume 186 - No.23, May 2024

A Semi-parallel Data Acquisition Method in Electrical Impedance Tomography using Undersampling Technique

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ABSTRACT

Hardware and software aspects of a semiparallel electrical impedance microtomography (EIT) system designed for high-speed data acquisition employing cost-effective measurements via subsampling techniques are covered in this paper. We explore the effects of the Nyquist theorem on sampling EIT system implementations through software and hardware testing. These experiments focus on the benefits of a semi-parallel approach, which involves serializing the excitation current and integrating parallelism into acquisition measurement hardware, operating under sub-Nyquist conditions. This innovative methodology promises greater efficiency and performance, potentially increasing the capabilities of EIT systems in diverse applications.

General Terms

Electrical impedance tomography, semi-parallel, undersampling

Keywords

Hardware implementation, semi-parallel, undersampling

1. INTRODUCTION

Electrical Impedance Tomography (EIT) is a well technique employed to characterizes the electrical properties of conductivity and permittivity of different materials. This technique is based on the spatial distribution of the electrical impedance, multi-measurement and processing process. A comprehensive system typically comprises two subsystems (i) hardware and (ii) software, as illustrated in Figure 1. Usually implemented on a general-purpose computer, the *software subsystem* assumes responsibility for tackling the inverse problem, thereby computing the impedance distribution. Within this subsystem, the impedance distribution is reconstructed, culminating in the formation of an image of the region of interest. The *hardware subsystem* is basically composed by a sensor and a control and acquisition unit. The sensor, tailored to specific applications, can be implemented using circular or planar electrode arrays, designed for either single (2D applications) or multilayer (3D applications) configurations. The control and acquisition unit assumes multiple roles, encompassing the generation, adaptation, conversion, and management of electrical current excitation signals for the emitting electrodes. Additionally, it handles the measurement, conditioning, filtering, and conversion of acquired electrical voltage signals.

Since the pioneering work of Barber and Brown[1] in 1989, which introduced the first Electrical Impedance Tomography (EIT) system, subsequent system proposals have predominantly relied on tetra-polar arrays for impedance distribution reconstruction. This involves conducting current injection and voltage measurement through pairs of distinct electrodes.

The coordination of electrical excitation and acquisition signals is commonly referred to as the excitation/measurement protocol, with the Adjacent/Neighbor Protocol emerging as the prevailing method. In this protocol, a pair of nearby electrodes serves as the current emitter, while all other adjacent pairs are designated for voltage measurement. Each electrode must, at least once, function as a transmitter, resulting in a total number of measurements given by

$$m = l(l-3), \tag{1}$$

where m is the number of measurements and l stands for the number of electrodes. The hardware strategies capable of changing these electrode arrangements can be categorized into serial architectures, parallel architectures, and semi-parallel architectures. Most EIT systems are based on series hardware architectures, in which a single current injection source and a single voltage measurement system block are responsible for the impedance distribution pattern [16, 18, 19]. This is possible by adopting a switching protocol for electrode selection as shown in Figure 2. These systems utilize switching devices to implement temporary switching

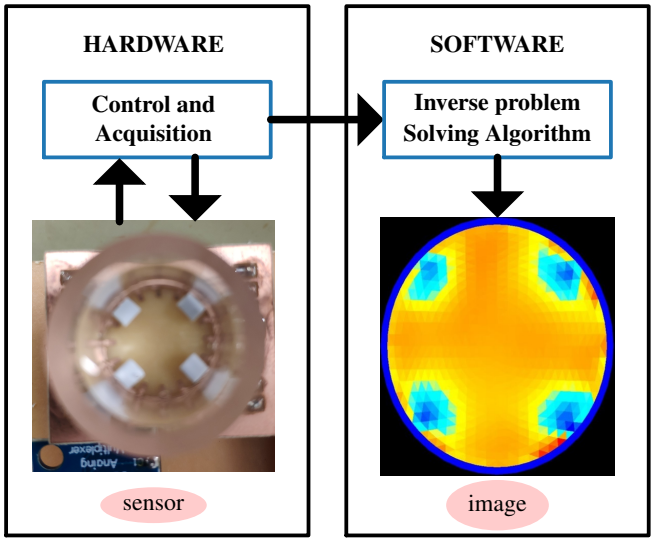

Fig. 1: Schematic diagram of an automatic multi-measurement sensor corresponding to a generic EIT system composed of hardware and software.

of current injection and voltage measurement. The action of switching devices, typically semiconductor-based analog multiplexers, introduces several implementation challenges. One such issue pertains to the contact resistance inherent in silicon-based devices, which can lead to voltage measurement errors exceeding acceptable thresholds for image reconstruction. Furthermore, the use of multiplexing devices can give rise to errors associated with stray capacitances [13], which impact on the reactive components of an EIT measurement. In addition to their influence on measurements, the main concern with switching devices lies in the switching time required for each measurement. This switching-time is influenced by both the dynamic characteristics of the multiplexer itself and the settling times of the signal processing sub-circuits. Consequently, these time intervals can culminate in a total measurement time that proves impractical for image reconstruction in certain applications. In a standard measurement circuit consisting of an active analog filter, signal amplifier and analog-to-digital converter, it typically takes an average of 13 seconds to acquire a single voltage measurement [16]. Extrapolating this acquisition duration to a system with 16 electrodes, as given in (1), results in a total acquisition time of more than 45 minutes. This long period highlights the main reason behind the widespread adoption of serial hardware systems: their inherent simplicity. By employing only one current injection subcircuit and one voltage measurement subcircuit, these systems simplify hardware complexity. Although accuracy and resolution considerations can impact the cost of these subsystems, such trade-offs are often acceptable, especially in applications where timestamp accuracy is not critical.

On the other hand, parallel hardware architectures avoid the need for electrode switching by employing multiple measurement and excitation subcircuits simultaneously. As comparatively represented in Figure 2, all electrodes remain active throughout the measurement process, facilitating the simultaneous injection of electrical current and the measurement of voltage across all pairs of electrodes. This parallel approach operates at multiple frequencies, requiring specific hardware and firmware characteristics. Pioneering this paradigm shift, the work of Oh *et al.* [12] proposed the KHU Mark2 hardware design, which incorporates a fully parallel EIT approach, implementing multiple current sources and voltage meters.

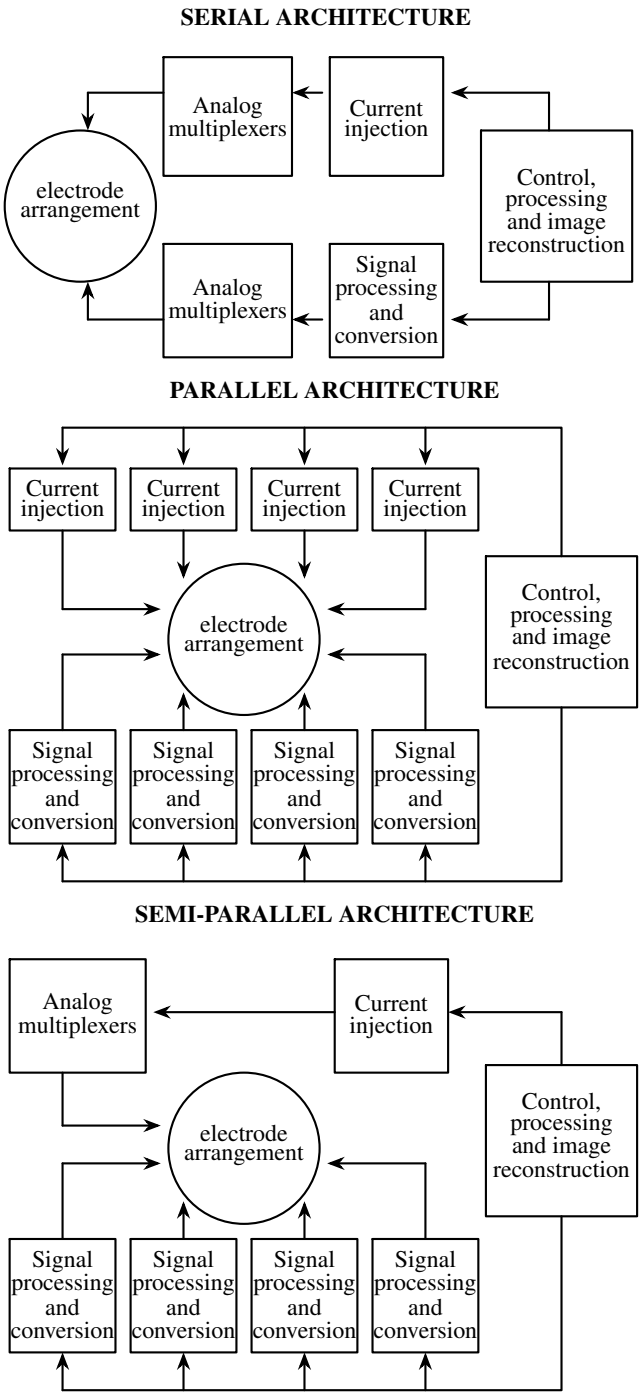

Fig. 2: Serial, parallel and semi-parallel EIT architectures.

This system achieves parallelism without relying on multiplexing devices, offering scalability of up to 64 electrodes and a sampling rate of 100 acquisitions per second. Although this approach enables real-time imaging and mitigates sources of error associated with multiplexing, its prohibitive costs and hardware density requirements make it impractical for many EIT applications.

1.1 Semi-parallel systems

An alternative to fully parallel measurement approaches involves solutions based on measurement parallelism (signal acquisition) and time-multiplexed current injection (excitation), resulting in intermediate characteristics compared to the systems mentioned above. Yunjie Yang and Jia [20] developed a fast multifrequency electrical impedance tomography (mfEIT) solution in this framework, where the switching of the electrodes in the array determines the pair associated with a frequency-adjustable current source. In contrast, all the other pairs of electrodes are simultaneously associated to independent signal acquisition and processing subcircuits partially implemented in field programmable gate arrays (FPGAs). A similar strategy with the feature that each acquisition and processing subcircuit is physically separated on different printed circuit boards (PCB) interconnected via a data bus using the CAN protocol, was followed by Miao *et al.* [9]. Frangi *et al.* [6] analyzed seven different architectures, characterized by serial injection and parallel measurement, calling them semi-parallel. Their research on measuring noise propagation using back-projection reconstruction concluded that this approach does not significantly compromise information retention compared to fully parallel architectures.
In a semi-parallel EIT architecture, as illustrated in Figure 2, although iterations related to injection switching are required, there is a performance improvement due to measurement parallelism compared to the serial approach. For example, while a series architecture with 16 electrodes requires 208 iterations, a semi-parallel architecture requires only 16 iterations. In particular, for all semi-parallel architectures examined, the correlation between performance, implementation cost, and parallelism of the measurement stage is maintained, with the signal processing and conditioning circuits being independent for each pair of electrodes. However, certain approaches resort to signal multiplexing at the input stage of the conversion, using a single analog-to-digital converter (ADC) to acquire information, as highlighted by Frangi [6]. This arises from the cost implications of implementing multiple ADCs with appropriate sampling and quantization resolutions for EIT signals. The lack of parallelism in the ADC conversion stage causes scalability problems and consequently constraints on the system's versatility.

2. DISCRETIZATION IN EIT SYSTEMS

As is well known in an EIT system, the fidelity of the reconstructed image is intrinsically linked to the quality of the impedance measurement [15]. This involves accurately measuring the magnitude (amplitude) of the voltage signal (*Vo*) and its phase shift to the reference signal (*Vr*) emitted by the source of electric current (see Figure 3). The robustness of these measurements is directly related to the effective quantification (resolution) and sampling (sampling rate) capabilities. Given the amplitude variations in signals sampled at different pairs of electrodes within an array, the resolution of ADCs in EIT systems typically exceeds 12 bits. Furthermore, temporal precision plays a key role in measuring signal phase and it is closely associated with the system's ability to faithfully reconstruct the original continuous signal information while adhering to the Nyquist-Shannon theorem [17].

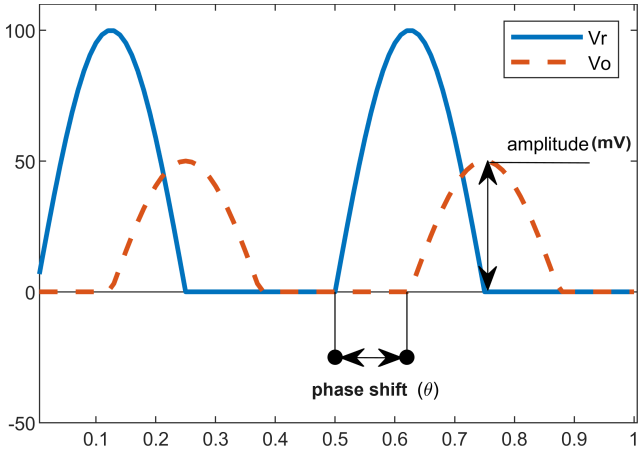

Fig. 3: Amplitude and phase-shift measurement parameters in an EIT system.

2.1 Nyquist–Shannon sampling theorem

The Nyquist-Shannon theorem and the discrete Fourier transform (DFT) are closely related concepts in signal processing, particularly in frequency sampling and analysis [17]. On the one hand, the Nyquist-Shannon theorem states that the minimum sampling frequency required to reconstruct a continuous signal must be at least twice the highest frequency component of the signal, known as the Nyquist frequency. On the other hand, DFT serves as a tool for analyzing the frequency content of discrete-time signals by transforming a sequence of sampled data points into their frequency-domain representation, thereby revealing the amplitude and phase of various frequency components within the signal. Furthermore, the Nyquist-Shannon theorem, also known as the sampling theorem, establishes the minimum criteria for sampling a band-limited periodic signal. It ensures effective discretization of a continuous signal by stipulating that the bandwidth B must be less than half the signal's uniform sampling rate f_s, that is, $B < \frac{f_s}{2}$, and that the occurrence of a signal $x(t)$ limited in band B has the sufficient condition for reconstruction from the samples at a uniform sampling rate f_s is $f_s > 2f(x)$. Meeting the Nyquist criteria is essential for signal discretization without aliasing or information loss, particularly in telecommunications. For example, in an electrical impedance tomography (EIT) system where the excitation frequency can vary, typically around 20kHz, the Nyquist theorem dictates that the sampling frequency of the ADC must exceed 40k samples per second. to accurately capture the signal. However, implementing ADCs with such high resolutions (e.g., 16 bits) and sampling rates (e.g., 40k samples per second) can be prohibitively expensive, making parallel conversion impractical.

2.2 Undersampling Technique

Undersampling, also known as *Sub-Nyquist* acquisition is a technique based on the fact that, despite frequency distortion (*aliasing*), the signal resulting from a sampling rate smaller than that proposed by Nyquist does not necessarily mean a loss of relevant information [8]. As an example, Figure 4 shows the result of an undersampling on a real 10Hz signal whose sampling is taken at a rate of 8.5 samples per second (sps). It is possible to observe that, although the original signal is described by

$$x(t) = 250 \cos 2\pi f t \tag{2}$$

with $f = 10$Hz. The resulting undersampling signal is described by

$$x_u(t) = 250 \cos 2\pi f_u t \quad (3)$$

where $f_u = 0.385$Hz stands for the undersampling or subsampling frequency. Although the result refers to an arbitrary sampling of high-frequency signals from the sub-Nyquist frequency band, the phase and amplitude are maintained in both signals $x(t)$ and $x_u(t)$, as long as the original frequency is known, all information relevant to the impedance calculation is available. The implementation of subsampling techniques, however, raises some problems already pointed out by Kerster [8], the main ones being in EIT are:
a) **Bandwidth of the sampled signal**: needs to be small enough to stay within the sub-Nyquist range without overlap. It is only relevant for multi-frequency systems.
b) **Limitations of the sample-and-hold circuit**: although subsampling allows signals to appear in digital space as low-frequency signals (sub-Nyquist frequency), they remain at high frequency in the analog domain. Thus, if the charge and discharge times of the capacitors in the sampling and retention circuits exceed the period of the signal, for example, the ADC will no longer be measuring the signal variation, even if subsampling theoretically allows it.
c) **Clock instability**: any instability in the ADC clock can result in noise in the measurement and, due to subsampling characteristics, the higher the subsampling rate, the greater the impact on the quality of the measured signal. Furthermore, clock drift over time causes the subsampled signals to shift in time, inducing a phase error between the signals.

3. UNDERSAMPLING EXPERIMENTS IN EIT SYSTEMS

The first work that addressed subsampling in EIT was the publication by Hartov [7] where a data acquisition system with 32 measurement channels with selectable multifrequency up to 1 MHz was proposed, built and evaluated. The implementation of subsampling was done through a technique called *Multiperiod Subsampling* based on the observation that, if the ratio between the sampling frequency and the frequency of the signal to be acquired is reduced to mutually prime factors, this ratio represents the number of unique samples during the number of periods. For example, when sampling an excitation signal of $f_s = 16.100$Hz, at a rate of 17sps, a sampling rate of 273.7ksps is required to obtain all acquisitions within the time interval of one period of the signal. However, considering that the sample is unique when it occurs at a specific time instant of a periodic signal, it is possible to obtain the same 17 samples of the f_s signal at a sampling rate of 136.85ksps, for two signal periods necessary for complete acquisition.
Based on this assumption and knowing the number of samples of interest to reconstruct the original signal, as well as the sampling rate of the acquisition system, it was possible to determine the minimum number of signal periods required to reconstruct each frequency f_s and the total acquisition time. It is remarkable that the described method has not been previously published in this context, despite being based on a technique already used in industrial electronics and measuring equipments. Among the precursors to the adoption of subsampling techniques are Dudykevych et al. [5] who present in their work the use of subsampling in impedance analyzers, in the context of spectroscopy and electrical tomography, and considering the non-idealization of sample blocks and signal retention present in ADC converters. The concept was validated by comparing theoretical and measured values in a functional prototype with different hardware blocks, called generator and analyzer,

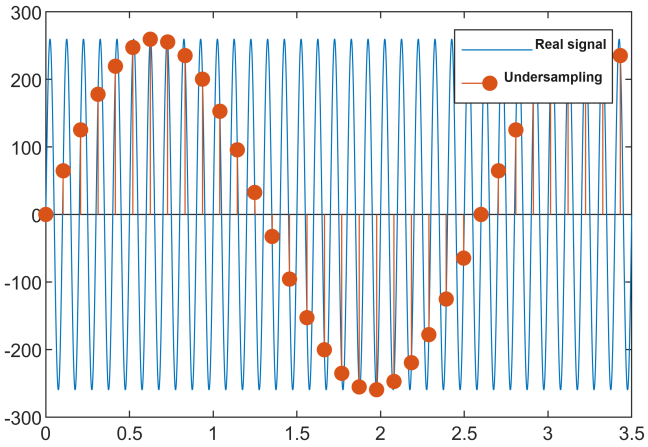

Fig. 4: An undersampling example of a sinusoidal signal, acquired in 8.5sps, where the real signal is $x(t)$ (in blue-color) and the undersampling signal corresponds to $x_u(t)$ (in red-color).

capable of obtaining the impedance values of a tetra-polar configuration.
The analyzer block uses ADC converters for current and voltage measurements with appropriate specific signal conditioning sub-blocks, followed by *FIFO* registers for connection to a Digital Signal Processor-DSP. The Programmable Gain Amplifier-PGA, Sampling and Retention-S/H and Analog-Digital Conversion-ADC sub-blocks are implemented in the aforementioned model AD9243 ADC converters which, according to the manufacturer, have an acquisition rate of 3 Msps. With the aforementioned acquisition rate, considering the *Nyquist* restrictions and the approach (see [21]) with the minimum number of acquisitions for recomposing an EIT signal, a theoretical excitation frequency not exceeding 375Khz is obtained. However, considering the SH sub-blocks of these ICs suitable for frequencies up to 20MHz, it was possible to implement subsampling techniques in the DSP resulting in the acquisition of drive frequencies up to 10Mhz with an impedance measurement accuracy of 0.012% in magnitude and 0.02° in phase. Based on the same technique, Wang *et al.* [18] developed his EIT system for online measurement of two-phase flows where an excitation frequency of up to 80 kHz can be measured with an error of less than 0.6% using the subsampling method, where all samples are acquired in a time interval of the excitation sine wave, originating from a pulse synthesizer block, with a fixed and precise phase shift between each sampling pulse. Min *et al.* [10] addressed the sampling of synchronized measurement and excitation signals applied in an algorithm developed and applied in DSP as an alternative to implementing undersampling, while Nagel *et al.* [11] present numerical synchronous detection as a theoretical alternative for bioimpedance measurement, where undersampling occurs through appropriately chosen integer multiples based on the excitation frequency. In another interesting paper, De Beer *et al.* [3] proposed the use of signal processing solutions through software implementations, increasing the bandwidth and dynamic range of a low-cost impedance analyzer, without the need for changes to *hardware*. Recent research in the last years has brought improvements in bandwidth through subsampling, and in the dynamic range through saturation, where it was possible to prove that the only limiting factor of the acquisition hardware is the amplifier bandwidth and the sampling and circuit times maintained by the digital-to-analog converter.

3.1 Software experiment

A data acquisition algorithm was implemented on an Arduino DUE platform, composed of an ARM Cortex-M3, using the integrated 12-bit ADC, to test the concept of subsampling. The process illustrated in the flowchart in Figure 5 aims to simulate two pseudo-parallel samples in the sub-Nyquist window with a temporal resolution of 1000sps. The multithreaded approach allows for analyzing the software scalability of multiple simultaneous measurements. Processes 1 and 2 are responsible for obtaining and maintaining samples from each converter independently, with a deliberate delay of 1ms between samples, while the main process sends all acquisition windows after the right number of samples (around 1.5 seconds per acquisition window). In this article, the signals were simulated in an arbitrary function generator model *Tektronix AFG1022*. Figure 6 presents the information from the two windows (processes) in a graph, showing half a wave of each signal (positive), while Table 1 shows the information corresponding to the original signal, provided by the two-channel arbitrary signal generator, and the signal resulting from the subsampling algorithm implemented as shown in Figure 5. It is possible to observe that the difference between the peak values of the measured signals and the original ones, or percentage error, is less than 0.5%. The attenuation in millivolts, that is, the difference between the peak voltage of channels 1 and 2, has an accuracy of 98.48% in the under-sampled signal. The phase-shift difference, however, is about 8.77% or 4 degrees. The reason for the high phase error is that although this test has pseudo-parallelism in the onboard processing, the hardware acquisition is a 12-bit multiplexed ADC [2]. This means that different software threads rely on input switching from a single analog-to-digital converter, accumulating runtime delays and preventing parallel processing.

Parameter	Value
Original frequency (Hz)	2001
Original period (s)	0,0004997
Original phase-shift (degrees)	45
Peak voltage in CH1-Measured (mV)	260
Peak voltage in CH2-Measured (mV)	128
Original attenuation (mV)	132
Sample interval (ms)	1
Undersampled frequency(Hz)	1,0965
Undersampled period (s)	0,912
Undersampled phase-shift (degrees)	48,94
Peak voltage in CH1-undersampled	258
Peak voltage in CH2-undersampled	128
Undersampled attenuation (mV)	130

Table 1. : Parameters of the first undersampling software experiment.

3.2 Hardware test

In order to avoid the phase shift error highlighted in 3.1, a new experiment was performed to prevent the multiplexing step in the analog-to-digital converter block. It is possible to solve the semi-parallelism problem mentioned above using a low-cost and high-resolution hardware resource in the quantization terms but with a sampling rate working in the sub-Nyquist band.

3.3 Parallel analog-do-digital conversion

The selected hardware resource was the AD7705 [4], an analog-digital front end for low-frequency measurement applications. Its performance is up to 16 bits of resolution using sigma-delta conversion and features a serial interface that can be configured for 3-wire operation. The topology of the AD7705 allows the user to apply an externally supplied oscillation frequency and, in this way, multiple devices can be synchronously powered by the same oscillator. To achieve 13-bit resolution or higher, the manufacturer recommends a sampling rate of less than 65sps. The second experiment uses the same multi-loop approach as the Arduino Due, including a new thread loaded to generate a 51Hz square wave. This signal is connected to the *MCLK IN* pin of two devices. Then, as a way to validate the possibility of obtaining subsampling data through the proposed approach, the parallel subsampling acquisition algorithm and hardware were integrated into the hardware data bus of a microEIT system [14], which allowed subsampling of data from the excitation and measurement signals from a real EIT measurement routine. The hardware assembly of the developed EIT system showing the 16-pole micro-sensor in the foreground is shown in Figure 7.

3.4 EIT measurement results

Experimental result corresponding to three subsampled measurements with the proposed microEIT system are shown in Figure 8. The information subsampled at time intervals of 500ms, from measurement protocol iterations number 13, 14, and 92, is shown in Figure 8, from top to bottom, respectively. The original frequency of the microEIT system works at 2kHz. The signal in red-color is related to the voltage between the injection electrodes, while the signal in blue-color corresponding to the measurement information from another pair of electrodes of the electrode array. In this figure one can observe the variation in phase-shift, as well as the attenuation between the two signals, related to the TIE measurement procedure.

4. CONCLUSIONS

The experiments presented in this work addressed subsampling techniques as a way of measuring with effective quantization through multiple ADC converters with high resolution and low sampling rate. As a consequence of this approach, the total implementation cost was considerably reduced with the proposed parallel measurement system. Temporal accuracy as an influencing factor in signal phase measurement is directly related to the scalability achievable with the embedded system architecture used for parallel signal data acquisition and processing. A system with simultaneous reading and processing of 16, 32 or 64 converter blocks implies a high implementation cost. In this sense, the subsampling technique with synchronization of ADC converters allows the economical implementation of a semi-parallel system in hardware, which can increase the performance and speed of data acquisition systems applied to EIT.

Future research activities should address the problem of scalability and pseudo-parallelism in a microprocessor, or of a high density of logic elements in a reconfigurable logic-based architecture to implement parallelism in measurement data acquisition. Approaches related to distributed systems, in the context of parallel measurement applied to TIE, can also be addressed in future research. Although processing implementation is the next step towards achieving a complete solution, the bench results from these experiments suggest that sub-Nyquist sampling in EIT systems is a promising approach to solving the trade-off between cost and parallelism, in terms of hardware implementation.

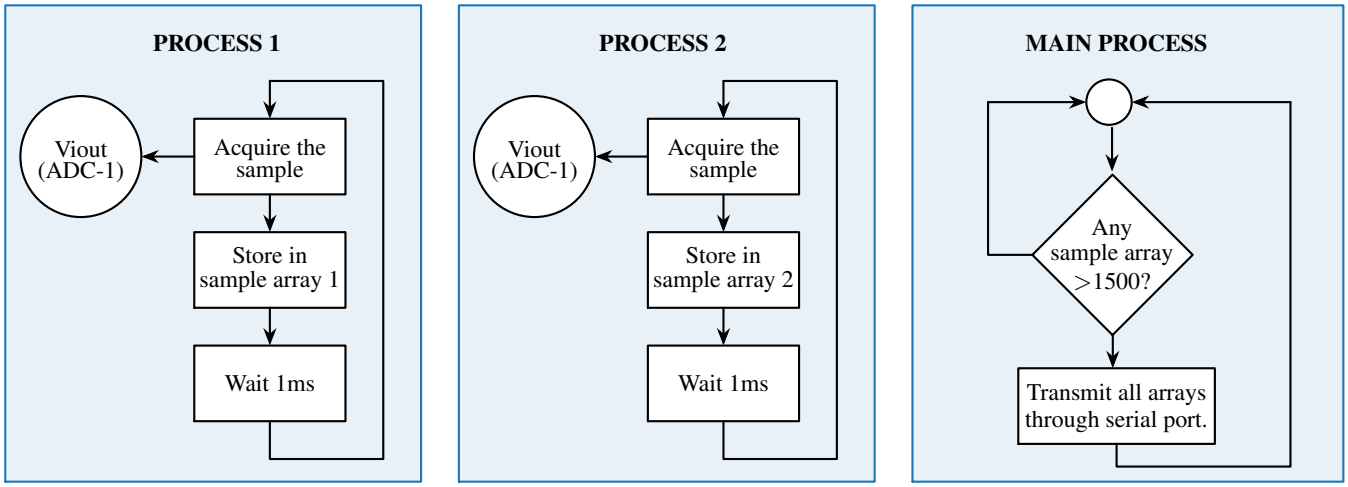

Fig. 5: Flowchart of the first test implemented in a multihead embedded platform.

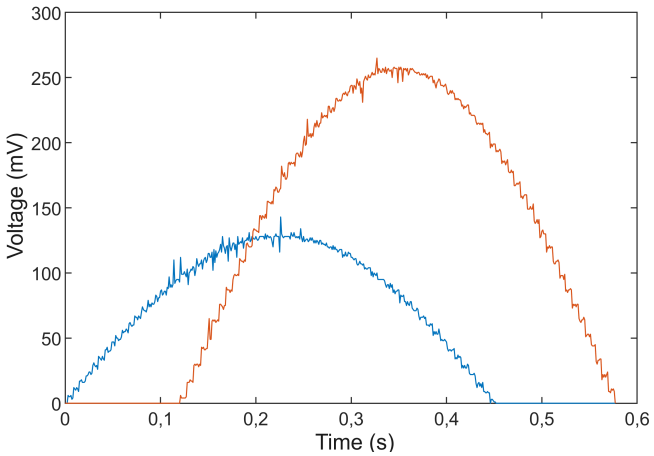

Fig. 6: Phase-shift between two half-wave signals in the first experimental test. Signal in red-color is related to the voltage between the injection electrodes. Signal in blue-color corresponding to the measurement information from a pair of electrodes in the array.

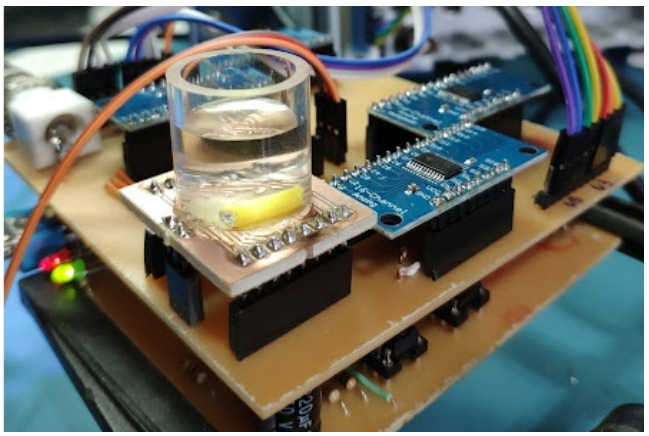

Fig. 7: Hardware assembly of the developed EIT system showing the 16-pole micro-sensor in the foreground.

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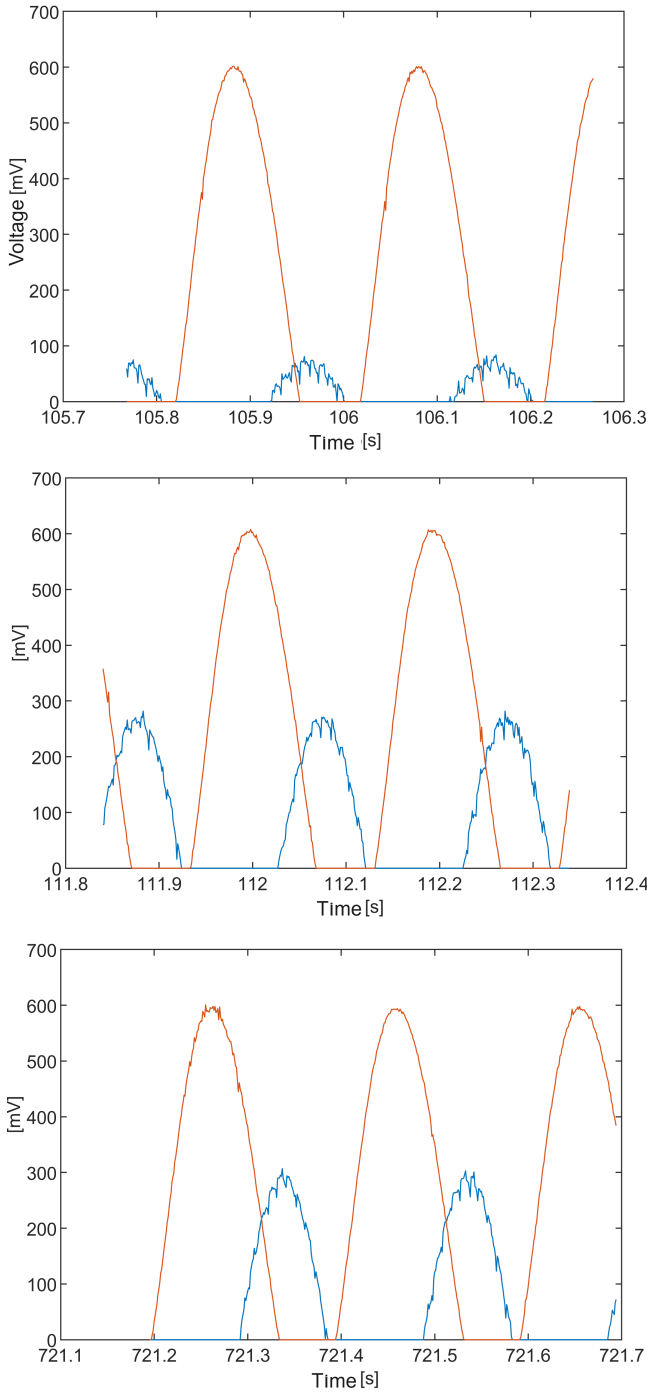

Fig. 8: Experimental result corresponding to three subsampled measurements (iterations numbers 13, 14, and 92, from top to bottom) with the proposed microEIT system.

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