Performance Study of Energy Recovery Logic and Conventional CMOS Full Adder

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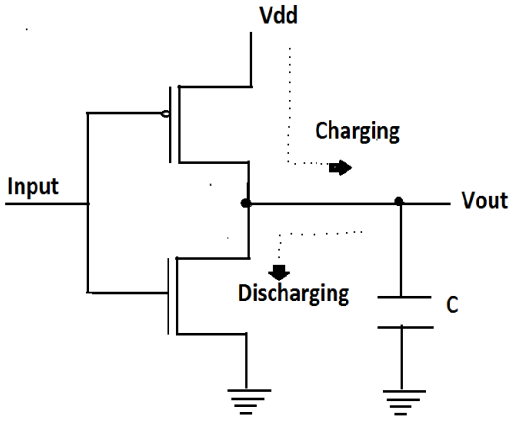
ABSTRACT
In recent times, there is huge demand of low energy and low voltage in electronics industry. This low power dissipation is very useful in wireless operated devices and in consumer electronics market or battery operated devices. These low power circuits have ability to reduce the battery cells and reduction in these cells can enhance the uses of low weight and tiny size systems. Authors have designed the combinational circuit full adder using adiabatic method ECRL and also done comparison with traditional CMOS in this paper. The energy recovery logic ECRL is reversible logic and it can minimize the power up to 70-75.Authors have also done number of analysis on adiabatic methodology like altering the frequency and rise time and fall time of the circuit. All the results and calculations are simulated on s-edit using TANNER v.7 technology.

Keywords
ECRL, CMOS, Full Adder. Adiabatic Logic

1. INTRODUCTION
The low power consumption is one of the main problem within the system SOC design.Eventhough the traditional CMOS have ability to reduce the energy dissipation up to some extent but not greater extent. In this method, different types of ways have been used like reduction in power supply, change in transistor width configuration, and reduce the value of node capacitance and combinations of all these parameters. In CMOS, basically three types of power consumptions are occurred. There are basically three types of power consumption in traditional CMOS such as Static, dynamic and short circuited power dissipation. In CMOS configuration, pull up and pull down network are used and most of the energy is dissipated in the pull up network and remained power is stored on capacitor [1].This stored charge is wasted in ground. But, it can be recycled back and used as power clock again. It is mention in thermodynamic process which is a reversible logic. The adiabatic logic is worked on this thermodynamic phenomenon and it can recover the partial or whole power from the load. In this paper, authors have designed the adiabatic full adder with ECRL which is partial energy recovery logic and their results are better than conventional CMOS [2].In section 1, adiabatic principle ECRL and conventional charging concept are discussed. Section 2 describes the circuit configuration of adiabatic full adder and conventional CMOS full adder with their description. Section 3 illustrates the simulated waveforms of the circuits. Section 4 shows the results and calculation using charts and graphs and Section 5 describe the conclusion.



"Fig 1: CMOS Process [1]."

1.1 Adiabatic Principle
The word ADIABATIC emanates from a Greek word that is utilized to show the thermodynamic process. In this phenomenon, energy does not mix with environment and there is no power loss across the node capacitance in the form of heat. But, in real time applications, this kind of process cannot be achieved due to the passive components such as resistors, capacitors. In spite of that, power dissipation of the circuit can be decreased by varying parameters like switching activity and power-delay product formula. Also, the energy stored on node capacitors can be reused as power clock. This adiabatic methodology is also called as Energy Recovery CMOS.As compared to conventional CMOS.This reversible logic works on pulsed power supply. During precharge and recovery phase, the charge is stored on node capacitance and recycled back to the source. The circuit whole power is conserved rather than dissipated as heat. This adiabatic logic is utilized according to the application and system specifications and digital systems can be loss free up to greater extent due to this reversible logic. The only half energy is dissipated in PMOSFET and remaining energy is recycled. The half energy is dissipated in R resistance of PMOS network. Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp [3].

Assume, the charging capacitor stored voltage V_C is zero initially.

The voltage across the switch = IR 1.1

P(t) in the switch = $I^2 R$ 1.2

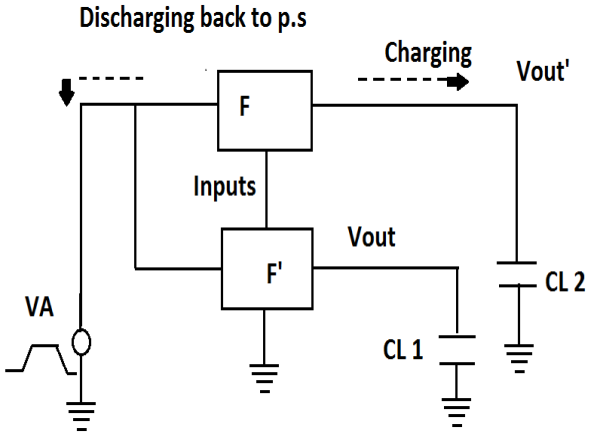
Energy during charge = $(I^2 R)T$ 1.3

E = $I^2 R = (CV|T)^2 RT = \frac{C^2 V^2}{RT}$ 1.4

$$E = E_{diss} = \frac{RC}{T} CV^2 = \frac{2RC}{T} \frac{1}{2} CV^2 \quad 1.5$$

The various parameters of equation (1.3) is describes below:

E — energy dissipated during charging time,
Q — total charge that stored on node capacitance,
C — value of the load capacitance,
R — on resistance of PMOS and NMOS,
V — output voltage at load,
T- time [4].



"Fig 2: Adiabatic Charging [5]."

From equation 1.3, basically two types of results can be found as given below:

(i) The energy which is dissipated as heat is always lesserthan the traditional CMOS condition.But,if the chargingtime period is greater than 2 RC.In other words, the dissipated power is less when the charging time period is increases.

(ii) The dissipated energy is directly proportional to the resistance R but it always opposite in conventionalCMOS. The dissipation in that case is entirely depend onthe capacitor C and voltage level.Moreover.the change in the on resistance of the PMOSFET can decrease the power consumption [5].

1.1.1. Types of Adiabatic Logic

1.1.1.1 Partially adiabatic logic. They are categorized as:

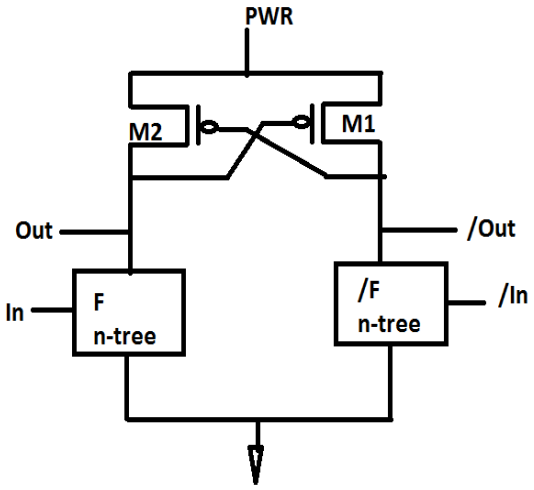
1) Efficient charge recovery logic (ECRL)
2) Quasi Adiabatic Logic (QAL)
3) Positive feedback adiabatic logic (PFAL)
4) 2N-2N2P Logic
5) True single phase adiabatic logic (TSAL)

1.1.1.2 Fully adiabatic logic. They are categorized as:

i) Pass transistor adiabatic logic
ii) Phase adiabatic Static CMOS logic (2PASCL)
iii) Split rail charge recovery logic (SCRL) [6].

1.1.2. ECRL Logic

Efficient Charge Recovery Logic (ECRL) proposed by Moon and Jeong.It uses cross-coupled PMOS transistors. It has the structure similar to Cascade Voltage Switch Logic (CVSL) with differential signaling, It consists of two cross-coupled transistors M_1 and M_2 and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block .It uses least number of transistors as compared to other logic familes.The two NMOS transistors are used for the purpose of logic functions. It does not require precharging diode and can minimize the energy dissipation. During transition of the constant power supply, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to $|V_{tp}|$, the PMOS transistor gets turned off [7].



"Fig 3: ECRL Logic [7]."

ECRL consist of pull up and pull down network. The pull up network is adiabatic latch and half of energy is dissipated in this network. The pull down network consists of two NMOS transistors and they can be worked as logic function. Both the networks are complement to each other. It operated on ramp power supply instead of DC supply due to its better performance in precharge and recovery phases. During tradition, the outputs out and out/ are charged with the constant energy of power supply and it is independent of the input signal level. When the signal level approaches to the peak value then the PMOSFETS is get turned off automatically [8].

2. FULL ADDER DESIGNS

2.1 Conventional CMOS Based Full Adder

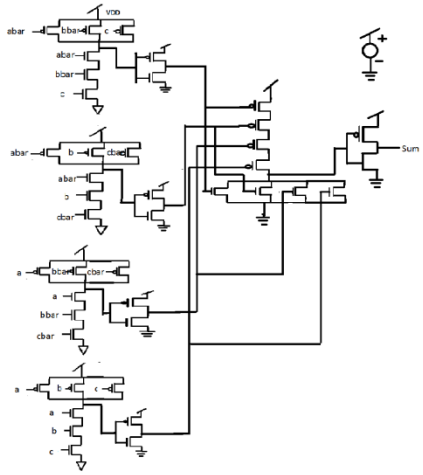
A TTL based full adder circuit is consist of three inputs binary signal a, b, cin and two outputs sum and carry. This adder is very simple to design and easy to understand but it has some limitations especially the power consumption and it span over the large area [9].

The power dissipation can be expressed by the following equation

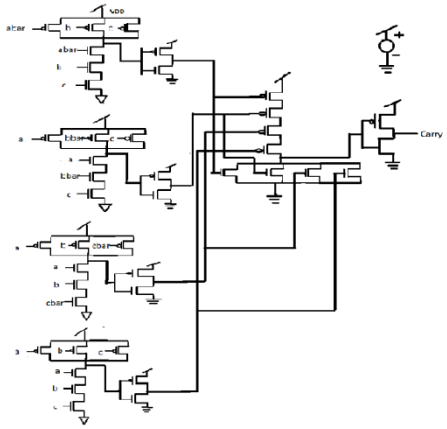
$$P = CV^2 f \quad 2.1$$

$$S = \overline{A}\ \overline{B}\ C + \overline{A}B\overline{C} + A\overline{BC} + ABC \quad 2.2$$

$$C = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC \quad 2.3$$



"Fig 4: CMOS Based Full Adder Sum [9]."

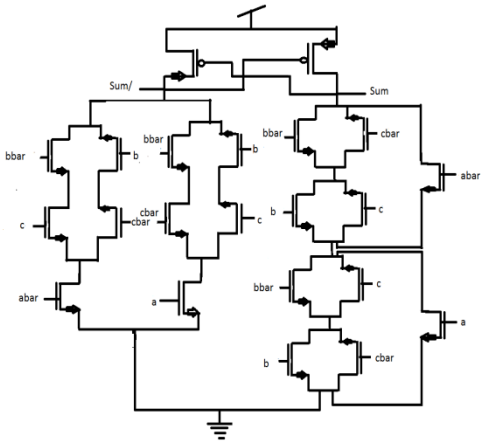


"Fig 5: CMOS Based Full Adder Carry [9]."

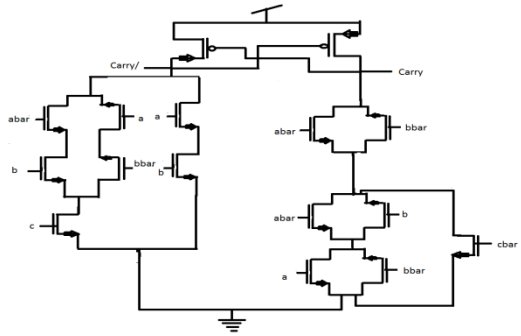
This methodology is implemented with AND, OR and NOT combination The half part generates the carry output and other half generates the sum output. The whole circuit is operated on DC power supply and produce huge power dissipation.

2.2 ECRL Based Full Adder

ECRL Logic is also called as cascade voltage switch logic with differential logic. The binary values are given in pull down network and these values are synthesis in this functional block. This block is purely made up of NMOS transistors. The pull up and pull down networks are work depending on the input logic level. The outputs sum, sum/, carry and carry/ retains the valid logic levels during hold phase of constant pulsed supply. During recovery phase, this logic value gives its energy to the power source back and can be reused. In other words, clock is work as power clock and power supply [10].



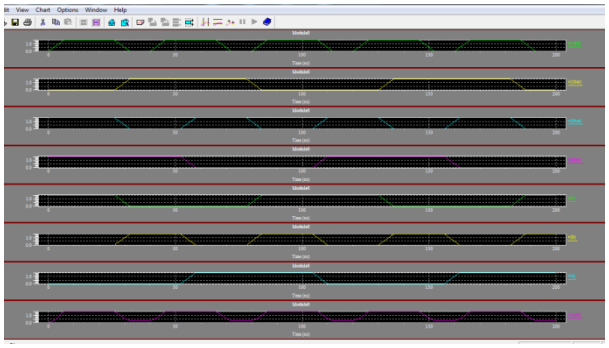
"Fig 6: ECRL Sum."



"Fig 7: ECRL Carry."

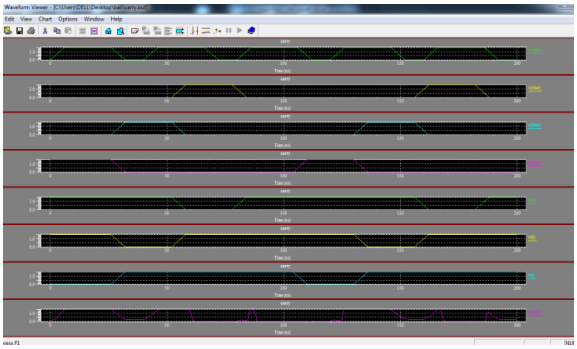
3. SIMULATED WAVEFORMS

In this paper, different kinds of logic styles are used for the designing of combinational full adder circuit in traditional and ECRL logic. All the waveforms are observed using s-edit of the TANNER V.7.The simulated waveforms of both logics are presented.



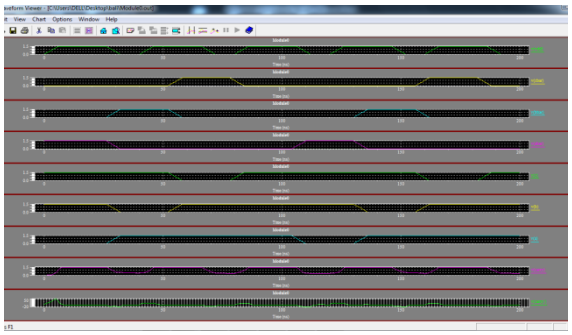
"Fig 8: Conventional CMOS Based Full AdderSum Simulated Waveforms".

Fig.8 verifies the logic behavior of conventional CMOS based full adder with simulated waveforms. The bottom one line represent the output signal sum and upper sevens are input signals.



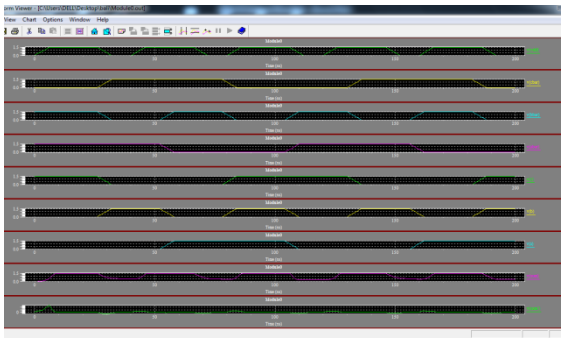
"Fig 9: Conventional CMOS Based Full AdderCarry Simulated Waveforms".

Fig. 9 verifies the logic behavior of conventional CMOS based full adder with simulated waveforms. The bottom one line represent the output signal carry and upper sevens are input signals.



"Fig 10: ECRL Based Full AdderSum Simulated Waveforms".

Fig. 10 verifies the logic behavior of ECRL based full adder with simulated waveforms. The bottom two lines represent the output signals sum and sum/ and upper sevens are input signals.

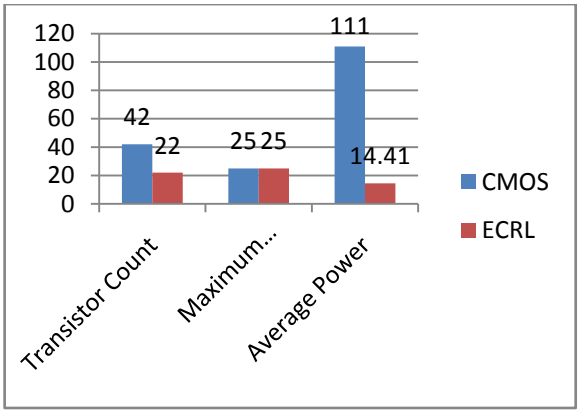


"Fig 11: ECRL Based Full Adder Carry Simulated Waveforms".

Fig. 11 verifies the logic behavior of ECRL based full adder with simulated waveforms. The bottom two lines represent the output signals carry and carry/ and upper sevens are input signals.

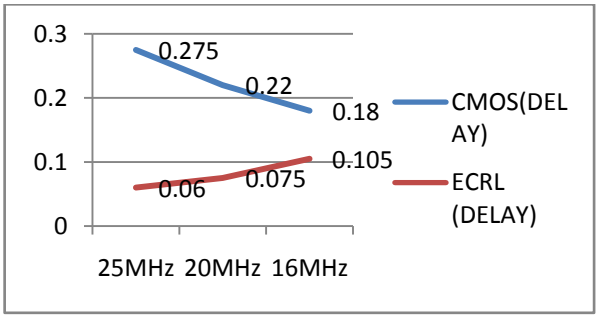
4. RESULTS &COMPARISON

In this graph, the dynamic power dissipated, transistor count and maximum frequency of CMOS and ECRL is shown in the fig.12.



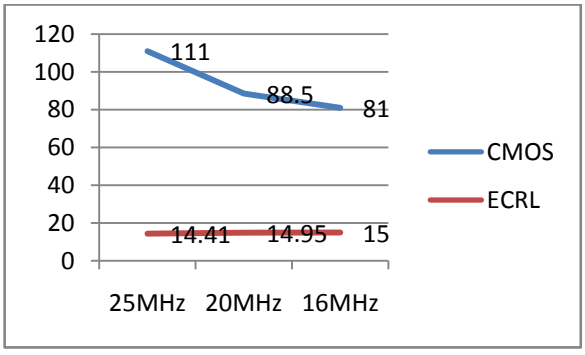
"Fig 12: Transistor Count, Max. Frequency andAvg. Power of Full Adder."

Fig.13 shows the variation in delay of the circuit with the change in the frequency. As the frequency decreases then the delay of CMOS and ECRL circuit is also decrease.



"Fig 13: Delay verses Frequency For Full Adder."

Fig.14 Shows the variation of power dissipated with the decrease in the frequency. At highest frequency, CMOSdissipated more power as compared to ECRL adder. Asthe frequency decreases the power is reduced by 81µwwith ECRL 15µw.



"Fig 14:Avg. power verses Frequency For Full Adder."

"Table1: Power dissipation results for full adder with frequency"

Frequency	Full Adder (CMOS)	Full Adder (ECRL)
16MHz	81µw	15µw
20MHz	88.5µw	14.95µw
25MHz	111µw	14.41µw

"Table1" shows the power consumption analysis of adiabatic circuit ECRL with conventional CMOS.The final results demonstrate that the energy dissipation of this reversible logic is least than conventional CMOS method.

"Table2: Average power dissipated, Maximum frequencyand transistor count of CMOS family and adiabatic logic ECRL based full adder circuit "

Parameters	Full Adder (CMOS)	Full Adder (ECRL)
Transistor Count	42	22
Maximum Frequency	25MHz	25MHz
Average power	111µw	14.41µw

"Table 2"shows the comparison analysis of various parameters such as transistor count, maximum frequency and average power dissipated of full adder.

"Table3: Delay verses frequency analysis for full adder

Frequency	Full Adder (CMOS)	Full Adder (ECRL)
16MHz	0.18s	0.105s
20MHz	0.22s	0.075s
25MHz	0.275s	0.06s

"Table 3" describe the delay verses frequency variations ofthe full adder with the different frequencies.

5. CONCLUSION

Authors have designed the full adder circuit with efficient charge recovery logic and conventional CMOS.A power consumption is reduced up to 14.41µw as compared to conventional CMOS with 111µw power consumption**.** All the parameters are simulated with tannerV7 on s-edit at 180nm technology. The adiabatic logic operated with pulsed power supplies of 1.5V which is very less as compared to 3.3V used in conventional CMOS.All calculations are verified at certain frequencies and temperature variations. Due to these performance parameters, this adiabatic approach is more convenient for energy efficient digital applications.

6. REFERENCES

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