

# Broadband Reconfigurable Low Noise Amplifier for Multiband Application

Bhavna Prajapati  
PG Scholar's NIIST

Swapnil Jain  
HoD EC  
NIIST BHOPAL

Braj Bihari Soni  
Asst Prof  
NIIST Bhopal

## ABSTRACT

In this paper Broadband Reconfigurable low Noise Amplifier for Multiband Application is presented. Low noise amplifier is versatile demanded in modern technology, technology demanded amplifier have less reflection and more rejection of noise, in this paper presented differential cross feedback topology and feedback technique for designing of Broadband Reconfigurable low Noise Amplifier, the requirement of integrated circuits raises significantly with increase in the number of elements in it. However, noise and reflection should be less. The noise content is based on the number of elements and routing of components and its process of fabrication. In this paper presented method to reduce noise contents with reduction of reflection. Significantly reducing noise figure (NF) to around 0.8 db, this paper present trade off between input and noise matching. The proposed LNAs achieve an NF of 0.1–0.8 dB over a impedance bandwidth of amplifier is 1GHz to 10 GHz.

## Keywords

Differential cross feedback topology; feedback topology; S11 Impedance bandwidth

## 1. INTRODUCTION

Advancements in IC technologies have improved analysis and realization of systems for a various of applications in the millimetre-wave bands. Especially, the availability of high-performance, Low-cost silicon technologies make it possible for such micro-systems to be commonly used in commercial products. Today, SiGe HBTs with maximum frequency of oscillation of 0.5 THz are available, creating the potential to demonstrate performance that is traditionally only available to III-V device technologies. As advancements in this field continue, a clear path is foreseen for devices with even higher speed. In this letter, we demonstrate a D-band low-noise amplifier (LNA) as a benchmarking circuit, realized in state-of-the art SG13G2 0.13 SiGe BiCMOS technology from IHP Microelectronics with HBTs providing of 300 GHz/500 GHz/1.6 V. The LNA utilizes an efficient Gain-boosting technique by inductive common-base termination. An analysis of this technique, the stability limit and an optimization methodology while maintaining stable operation is provided within this letter. The results demonstrate state-of-the-art performance, exceeding LNAs realized in other silicon-based technologies in this frequency range.

## 2. PROPOSED DESIGN ANALYSIS

The proposed designing depict in fig 1, due to differential mode configuration biasing arrangement is not required. The parasitic effects of RF coil and capacitor are also considered in the design. In cross dual-feedback a CG LNA design, the boosted feedback utilizes the capacitor cross-coupled (CCC) technique, Moreover; a superior is achieved using a differential amplifier configuration. Therefore, the input matching condition for proposed LNAs is achieved, where denotes differential input impedance. Additionally, the positive feedback is constructed using a Inductor, inductive feedback technique is used for improvement of impedance bandwidth, the circuit diagram of the proposed three-stage Broadband Reconfigurable low Noise Amplifier is shown in Fig. 1. The Broadband Reconfigurable low Noise Amplifier. consists of an input balun with three switched capacitors, two series driver stages (DS1 and DS2), two shunt power stages (PS). The transistor sizes determined by the emitter area, this Broadband Reconfigurable low Noise Amplifier. in class AB for good linearity and efficiency. Compared to the other Pas using a PCT at the gigahertz band and 0.18- m CMOS process [26], [27], our proposed structure presents the wider operating bandwidth. consisting of two transistors ( and ) and passive components ( and ) are employed in the bases of DS1, DS2, and PS to function as linearizers [28]. The differential configuration of individual driver and power stages produces a virtual ground, which avoids the emitter degeneration effect of grounding bond wires. Additionally, the differential topology reduces self-mixing of even-mode harmonics with the fundamental signal, shows that the tuning at the input balun achieves frequency-independent power contours over operating bands. To demonstrate the usefulness of tuneable, when is tuning at different operating bands. Moreover the advantage of the proposed tuneable is further demonstrated by differential networks at the input port of the Broadband Reconfigurable low Noise Amplifier.. configurations are presented in Table II. Results validate that our proposed tuneable with compact size possesses wider operating bandwidth and lower loss than those of the single-stage and multi-stage matching networks. To compensate the matching network loss,

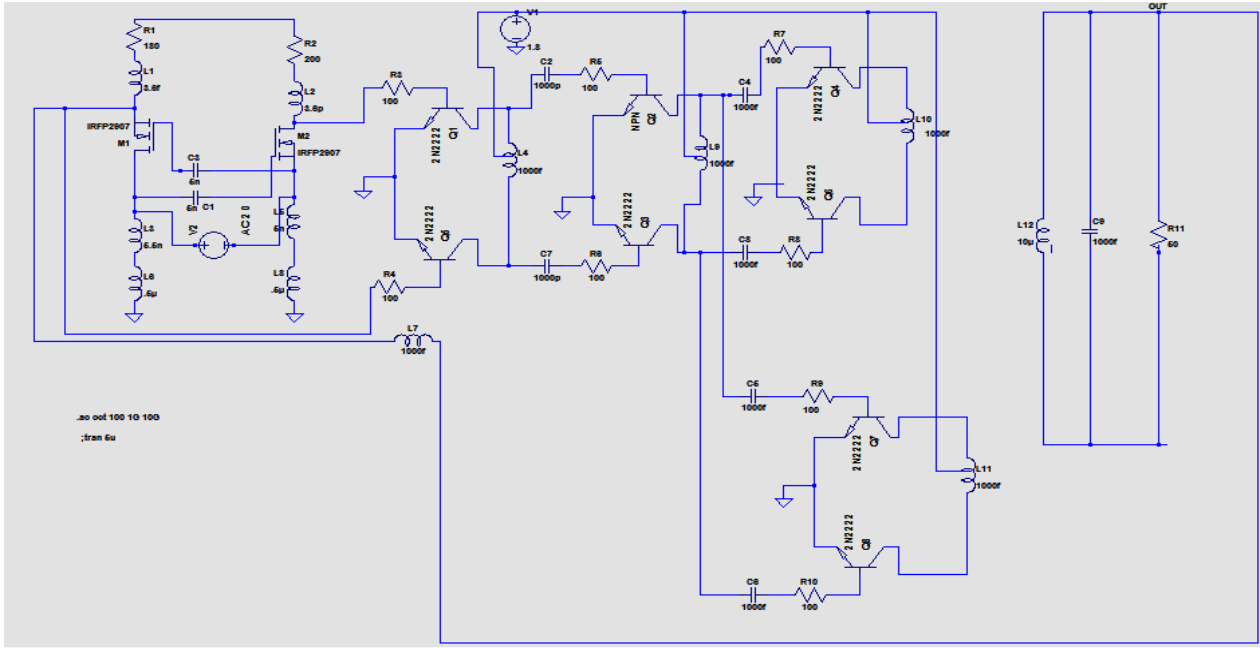


Fig 1 Proposed Amplifier

### 3. RESULT DISCUSSION

The proposed design is design and validated in LT-Spice simulator, the S-Parameters of proposed design shown in Fig. 2. The proposed LNA achieves a  $S_{11} \leq -14$ dB, between 1-10GHz. The objective of the proposed work is to design an amplifier with broad impedance matching with less contain of noise. Fig. 1 shows the schematic of the proposed Broadband Reconfigurable low Noise Amplifier. This amplifier design for 1GHz to 10GHz application. First stage consists of differential mode amplifier to provide high input impedance. In second stage used cross feedback topology using capacitor technique to improve impedance bandwidth of amplifier, the design of all elements according to resonance theory, to reduce the noise figure induced feedback inductor; high mobility NMOS transistor is preferred in the design of amplifier. The optimum 1.8 V gives very good linearity, the optimization of the proposed Design is design as per as required bandwidth, gain, and noise figure, It should be noticed that equivalent inductance consider because of the feedback mechanism and series inductance and internal capacitive of MOSFET, this create impedance matching network and gives broad band impedance matching. Overall improves input impedance matching and reduce reflection of proposed design, the second circuit are used to further extend the bandwidth using inductive feedback technique. The feedback inductor is sized to 1mH so that its parasitic capacitance due to the output stage would not cause reflection degradation at tens of GHz range. According to

noise analysis minimum NF as possible over the entire bandwidth 1 to 10GHz, Simultaneously obtain input noise and output noise. Similarly, the value determines the final voltage gain once the wideband input and noise matching as been done. the value of elements is finally chosen to satisfy the high linearity requirement. High gate charge transistor and minimum value of  $R_{on}$  is used to reduce reflection and noise contents However, the linearity issue should be addressed because a larger reduction of noise contents. Shielding structures have been realized on the metal-insulator-metal capacitors and RF coil to reduce the noise coupling through the substrate. While operating at a supply voltage of 1.8 V,

The external wideband baluns are used to convert between single-ended and differential signals in the measurement. Notably, the loss of wideband baluns needs to be de-embedded beforehand. Cross dual-feedback LNAs design using capacitor.

The validation results of proposed amplifier are discussed in next section.

#### 3.1 S11 Reflection analysis

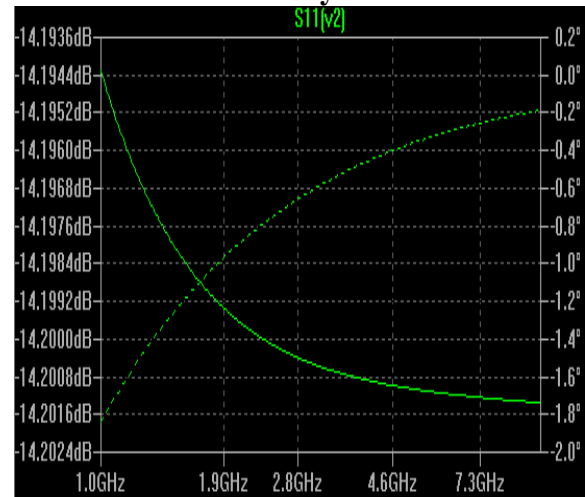


Fig 2 Simulated S11-parameters

The simulated results of S11 is shown in fig 2, the reflection is reduce significantly from 1GHz to 10GHz. Achieved  $S_{11} \leq -14$ dB, from 1GHz to 10GHz for input port.

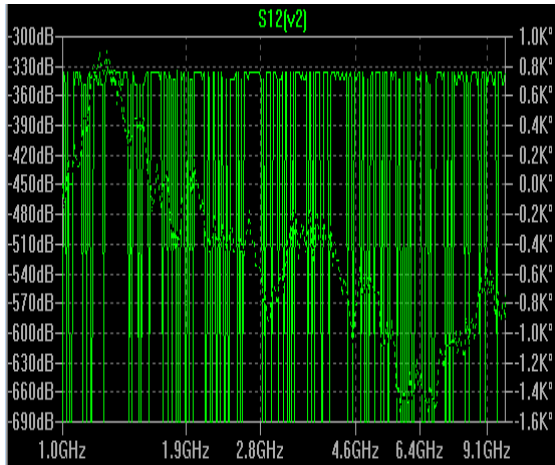


Fig 3 Simulated S22 -parameters

The simulated results of S22 is shown in fig 3, the reflection is reduce significantly from 1GHz to 10GHz. Achieved S22  $\leq$  -300dB, from 1GHz to 10GHz.

### 3.2 Input and Output Voltage analysis

The input and output voltage analysis is shown in fig 4, from this analysis concluded that loss of signal is very small obtain similar value of input and output voltage.

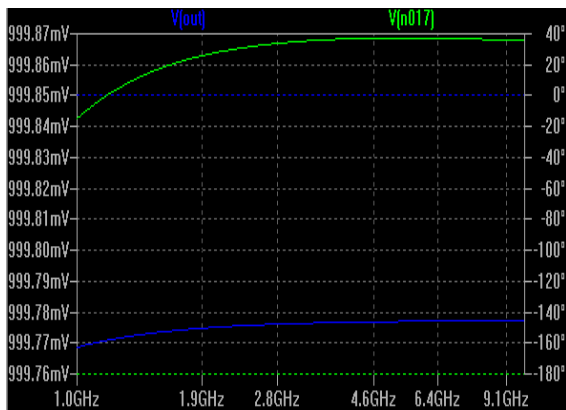


Fig 4 Input and Output Voltage analysis

### 3.3. Input and Output Current Analysis

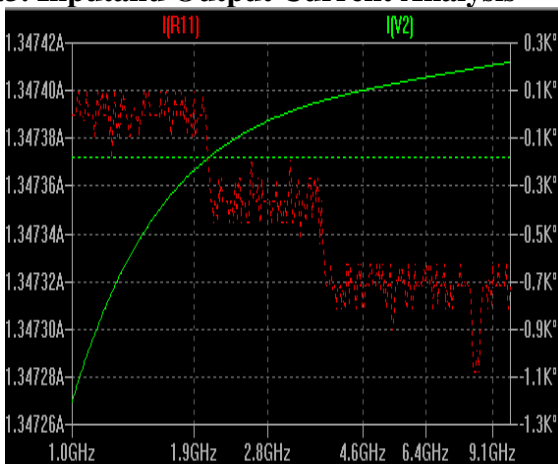


Fig 5 input and output current analysis

The input and output current analysis is shown in fig 5, from this analysis concluded that loss of signal is very small obtain

amplification of current in the frequency range of 1GHz to 2GHz, similar value of input and output current with small loss of current obtain from 2.1GHz to 10GHz.

### 3.4. Noise Analysis

Noise analysis is a important and demanded in designing of recent amplifier in section a. input noise analysis is given and in section b. out noise analysis is given.

#### 3.4.1. Input noise analysis

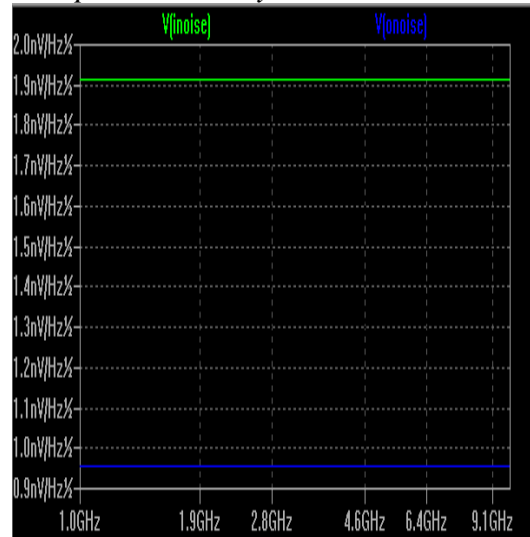


Fig 6 Input and output noise analysis

Input noise input in amplifier using source is up to 1.9nV/ $\sqrt{\text{Hz}}$ . Input noise with respect to frequency is shown in fig 5

#### 3.4.2. Output noise analysis

Out noise analysis is shown in fig 6, from this fig concluded that noise in output of amplifier obtain 0.9nV/ $\sqrt{\text{Hz}}$  flat over the frequency range of 1GHz to 10GHz, the noise figure of amplifier define as

$$\text{Noise Figure} = 10 \log \frac{\text{Output Noise}}{\text{Input noise}}$$

Obtain Noise Figure up to .1 to .8dB,

### 3.5. Group delay

Table 1 Comparison of Proposed Work with Literatures

Reference Paper	Year	Journal & Author	Technology	S11 (dB)	Bandwidth (GHz)	NF (dB)	Power consumption
[2]	2015	IEEE Journal	0.18 $\mu$ m BiCMOS	$\leq -7$	110-140	5.5-4.5	12mw
This Work			0.18 $\mu$ m CMOS	$\leq -14$	1 - 10	0.1 to 0.8	0.003

### 4. CONCLUSION

This paper has proposed a fully monolithic three-stage Broadband Reconfigurable low Noise Amplifier for WCDMA, and WLAN applications in 0.18- m SiGe BiCMOS technology. To improved linearity in inside of amplifier a tuneable input matching network, a broadband transformer-type output matching network, used in power amplifier, the input tuneable matching network consisting of a balun. A 1-10 GHz Broadband Reconfigurable low Noise Amplifier is presented, the designing of proposed amplifier and analysis carried out in LT-Spice simulator.

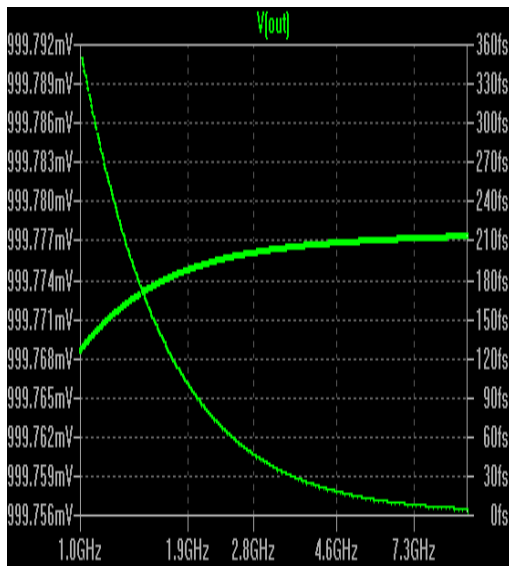


Fig 7 Group delay of amplifier

The group delay of amplifier is shown in fig 7; the proposed amplifier has very less propagation delay from 36fsec to 0fsec for reduction in noise and reflection with improved linearity of amplifier. The validation of work is shown in table –1, compare the work with previous work, with respect to noise figure, S11 Bandwidth and frequency of application.

Validation of work is shown in Table-I, simulation done from 1-10GHz. From this validation concluded that proposed amplifiers have better performance compare to previous work with respect to S11 bandwidth, noise figure and power dissipation,

A differential mode cross capacitive feedback technique, feedback inductive gives very good input and out matching over a large bandwidth. a minimum 0.1 from 1GHz to 10GHz. The proposed amplifier presents a broad bandwidth. This work involves designing two CMOS common gate LNAs with different cross dual-feedback techniques to attain good input matching, low NF, and high linearity over a wide frequency range. With the dual feedback, CG LNA adds a degree of

freedom in the design to relieve a difficult trade-off between input and noise matching, further uses the secondary winding

coil of the transformer to perform series peaking. the reflection is reduce significantly from 1GHz to 10GHz. Achieved  $S_{22} \leq -300$ dB, from 1GHz to 10GHz. from this analysis concluded that loss of signal is very small obtain amplification of current in the frequency range of 1GHz to 2GHz, similar value of input and output current with small loss of current obtain from 2.1GHz to 10GHz. Achieved  $S_{11} \leq -14$ dB, from 1GHz to 10GHz for input port. Concluded that loss of signal is very small obtaining similar value of input and output voltage.

### 5. REFERENCES

- [1] Ming-Lung Lee, Chong-Yi Liou, Student Member, IEEE, "Fully Monolithic BiCMOS Reconfigurable Power Amplifier for Multi-Mode and Multi-Band Applications" IEEE transactions on microwave theory and techniques, VOL. 63, NO. 2, February 2015 pp 613-624
- [2] Çağrı Ulusoy, Member, "A SiGe D-Band Low-Noise Amplifier Utilizing Gain-Boosting Technique" IEEE Microwave And Wireless Components Letters, VOL. 25, NO. 1, January 2015 pp 61-66
- [3] Jongwon Lee, Jooseok Lee, and Kyoungsoon Yang, Senior Member, IEEE "Reflection-Type RTD Low-Power Amplifier With Deep Sub-mW DC Power Consumption" IEEE Microwave And Wireless Components Letters, VOL. 24, NO. 8, August 2014 pp 551-553
- [4] V. Giannini, P. Nuzzo, et.al Dec. 2009. "A 2 mm 0.1-to-5 GHz SDR receiver in 45 nm digital CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 12, pp. 3486–3498,
- [5] R. van de Beek et.al, Feb. 2008 "A 0.6-to-10 GHz receiver front-end in 45 nm CMOS," in IEEE Int. Solid-State Circuits Conf. Tech. Dig., pp. 128–129.
- [6] B. G. Perumana, et.al. May 2008. "Resistive-feedback CMOS low-noise amplifiers for multiband applications," IEEE Trans. Microw. Theory Techn., vol. 56, no. 5, pp.1218–1225.
- [7] M. T. Reiha and J. R. Long, May 2007. "A 1.2V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 m CMOS," IEEE J. Solid-State Circuits, vol. 42, no. 5, pp. 1023–1033.
- [8] R.-M. Weng, C.-Y. Liu, et.al, Aug. 2010. "A low-power full-band lownoise amplifier for ultra-wideband receivers," IEEE Trans. Microw. Theory Techn., vol. 58, no. 8, pp. 2077–2083.
- [9] J.-F. Chang et.al, May 2011. "0.99 mW 3–10 GHz common-gate CMOS UWB LNA using T-match input network and self-body-bias technique," Electron. Lett., vol. 47, no. 11, pp. 658–659.

- [10] B. Park, S. Choi, Jan. 2010., “A low-noise amplifier with tunable interference rejection for 3.1- to 10.6-GHz UWB systems,” *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 1, pp. 40–42.
- [11] K.-H. Chen, J.-H. Lu, et.al, Mar. 2007. “An ultra-wide-band 0.4–10-GHz LNA in 0.18- m CMOS,” *IEEE Trans. Circuits Syst. II,Exp. Briefs*, vol. 54, no. 3, pp. 217–221.
- [12] Y.-T. Lo and J.-F. Kiang, Sep. 2011. “Design of wideband LNAs using parallel-to series resonant matching network between common-gate and common source stages,” *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 9, pp.2285–2294.
- [13] D. Pepe and D. Zito, Sep. 2009. “22.7-dB gain 19.7-dBm UWB CMOS LNA,” *IEEE Trans. Circuits Syst. Exp. Briefs*, vol. 56